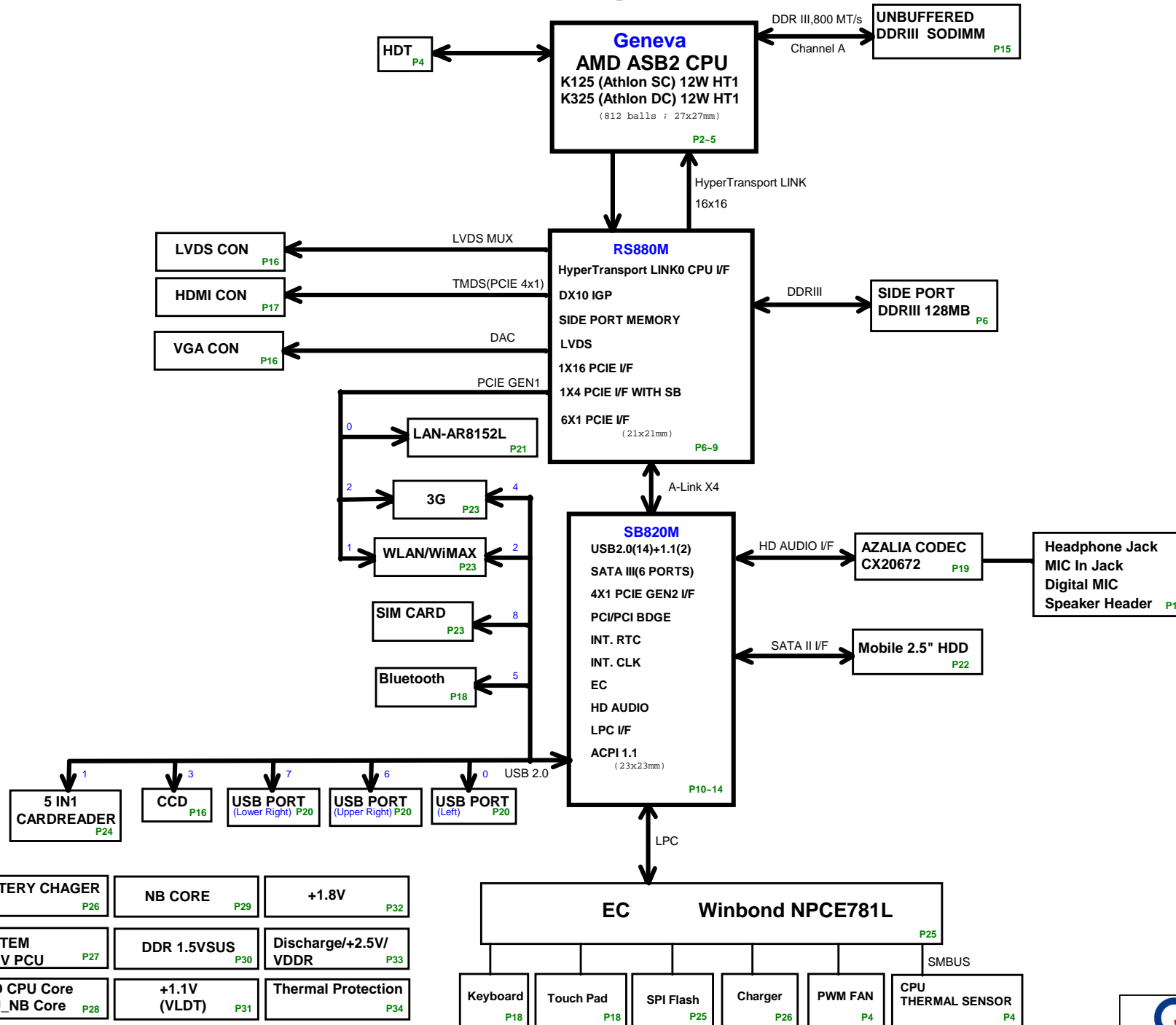














# ZH9 Block Diagram (AMD Nile Platform)



<6> HT\_CADINP[15..0]  HT\_CADINP[15..0]  
 <6> HT\_CADINN[15..0]  HT\_CADINN[15..0]  
 <6> HT\_CLKINP[1..0]  HT\_CLKINP[1..0]  
 <6> HT\_CLKINN[1..0]  HT\_CLKINN[1..0]  
 <6> HT\_CTLINP[1..0]  HT\_CTLINP[1..0]  
 <6> HT\_CTLINN[1..0]  HT\_CTLINN[1..0]  
 <6> HT\_CADOUTP[15..0]  HT\_CADOUTP[15..0]  
 <6> HT\_CADOUTN[15..0]  HT\_CADOUTN[15..0]  
 <6> HT\_CLKOUTP[1..0]  HT\_CLKOUTP[1..0]  
 <6> HT\_CLKOUTN[1..0]  HT\_CLKOUTN[1..0]  
 <6> HT\_CTLOUTP[1..0]  HT\_CTLOUTP[1..0]  
 <6> HT\_CTLOUTN[1..0]  HT\_CTLOUTN[1..0]

U16A			
HT_CADINP15	W7	L0_CADIN_H15	L0_CADOUT_H15
HT_CADINP15	W6	L0_CADIN_L15	L0_CADOUT_L15
HT_CADINP14	U6	L0_CADIN_H14	L0_CADOUT_H14
HT_CADINP14	U5	L0_CADIN_L14	L0_CADOUT_L14
HT_CADINP13	R7	L0_CADIN_H13	L0_CADOUT_H13
HT_CADINP13	R6	L0_CADIN_L13	L0_CADOUT_L13
HT_CADINP12	P6	L0_CADIN_H12	L0_CADOUT_H12
HT_CADINP12	P5	L0_CADIN_L12	L0_CADOUT_L12
HT_CADINP11	L6	L0_CADIN_H11	L0_CADOUT_H11
HT_CADINP11	L5	L0_CADIN_L11	L0_CADOUT_L11
HT_CADINP10	J6	L0_CADIN_H10	L0_CADOUT_H10
HT_CADINP10	J5	L0_CADIN_L10	L0_CADOUT_L10
HT_CADINP9	H4	L0_CADIN_H9	L0_CADOUT_H9
HT_CADINP9	H3	L0_CADIN_L9	L0_CADOUT_L9
HT_CADINP8	G6	L0_CADIN_H8	L0_CADOUT_H8
HT_CADINP8	G5	L0_CADIN_L8	L0_CADOUT_L8
HT_CADINP7	T3	L0_CADIN_H7	L0_CADOUT_H7
HT_CADINP7	T4	L0_CADIN_L7	L0_CADOUT_L7
HT_CADINP6	T2	L0_CADIN_H6	L0_CADOUT_H6
HT_CADINP6	T1	L0_CADIN_L6	L0_CADOUT_L6
HT_CADINP5	P3	L0_CADIN_H5	L0_CADOUT_H5
HT_CADINP5	P4	L0_CADIN_L5	L0_CADOUT_L5
HT_CADINP4	P2	L0_CADIN_H4	L0_CADOUT_H4
HT_CADINP4	P1	L0_CADIN_L4	L0_CADOUT_L4
HT_CADINP3	M2	L0_CADIN_H3	L0_CADOUT_H3
HT_CADINP3	M1	L0_CADIN_L3	L0_CADOUT_L3
HT_CADINP2	K3	L0_CADIN_H2	L0_CADOUT_H2
HT_CADINP2	K4	L0_CADIN_L2	L0_CADOUT_L2
HT_CADINP1	K2	L0_CADIN_H1	L0_CADOUT_H1
HT_CADINP1	K1	L0_CADIN_L1	L0_CADOUT_L1
HT_CADINP0	H2	L0_CADIN_H0	L0_CADOUT_H0
HT_CADINP0	H1	L0_CADIN_L0	L0_CADOUT_L0
HT_CLKINP1	M8	L0_CLKIN_H1	L0_CLKOUT_H1
HT_CLKINP1	M7	L0_CLKIN_L1	L0_CLKOUT_L1
HT_CLKINP0	M3	L0_CLKIN_H0	L0_CLKOUT_H0
HT_CLKINP0	M4	L0_CLKIN_L0	L0_CLKOUT_L0
HT_CTLINP1	Y6	L0_CTLIN_H1	L0_CTLOUT_H1
HT_CTLINP1	Y5	L0_CTLIN_L1	L0_CTLOUT_L1
HT_CTLINP0	V2	L0_CTLIN_H0	L0_CTLOUT_H0
HT_CTLINP0	V1	L0_CTLIN_L0	L0_CTLOUT_L0
HT_CADOUTP15	AB6	HT_CADOUTP15	HT_CADOUTN15
HT_CADOUTP15	AB5	HT_CADOUTP14	HT_CADOUTN14
HT_CADOUTP15	AB4	HT_CADOUTP13	HT_CADOUTN13
HT_CADOUTP15	AC7	HT_CADOUTP12	HT_CADOUTN12
HT_CADOUTP15	AC6	HT_CADOUTP11	HT_CADOUTN11
HT_CADOUTP15	AE6	HT_CADOUTP10	HT_CADOUTN10
HT_CADOUTP15	AE5	HT_CADOUTP9	HT_CADOUTN9
HT_CADOUTP15	AK3	HT_CADOUTP8	HT_CADOUTN8
HT_CADOUTP15	AK4	HT_CADOUTP7	HT_CADOUTN7
HT_CADOUTP15	AH2	HT_CADOUTP6	HT_CADOUTN6
HT_CADOUTP15	Y1	HT_CADOUTP5	HT_CADOUTN5
HT_CADOUTP15	Y2	HT_CADOUTP4	HT_CADOUTN4
HT_CADOUTP15	Y4	HT_CADOUTP3	HT_CADOUTN3
HT_CADOUTP15	Y3	HT_CADOUTP2	HT_CADOUTN2
HT_CADOUTP15	AB1	HT_CADOUTP1	HT_CADOUTN1
HT_CADOUTP15	AB2	HT_CADOUTP0	HT_CADOUTN0
HT_CADOUTP15	AD1	HT_CLKOUTP1	HT_CLKOUTN1
HT_CADOUTP15	AD2	HT_CLKOUTP0	HT_CLKOUTN0
HT_CADOUTP15	Y8	HT_CTLOUTP1	HT_CTLOUTN1
HT_CADOUTP15	Y9	HT_CTLOUTP0	HT_CTLOUTN0
HT_CADOUTP15	V4	HT_CTLOUTP1	HT_CTLOUTN1
HT_CADOUTP15	V3	HT_CTLOUTP0	HT_CTLOUTN0

HT LINK

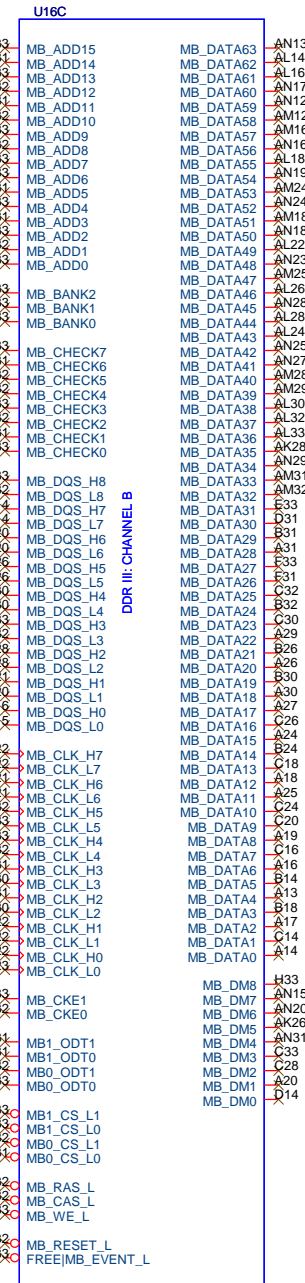
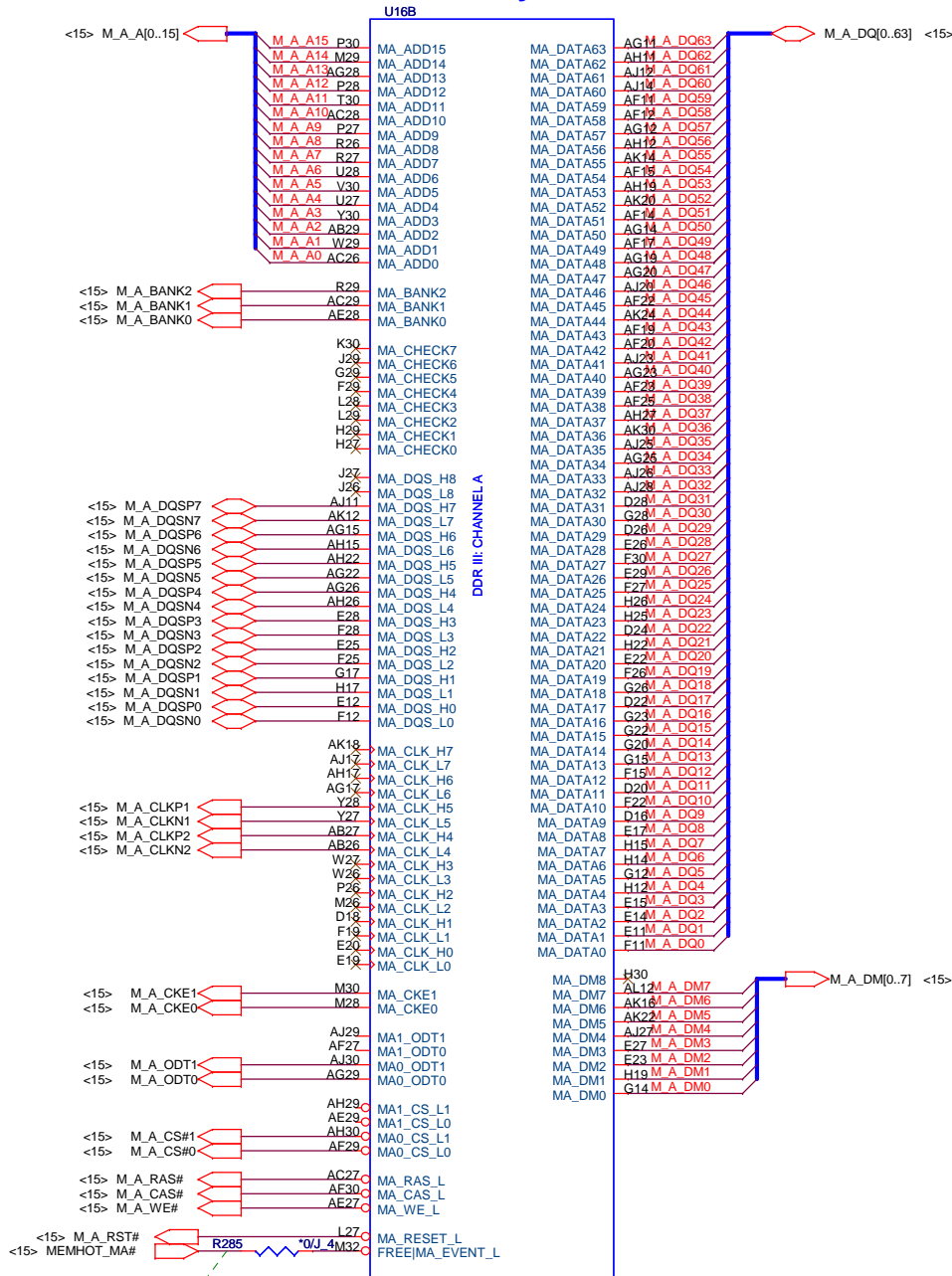


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PROJECT : ZH9

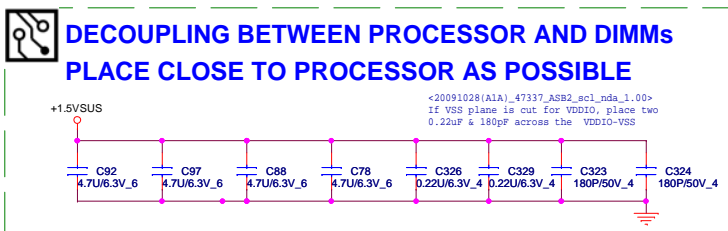
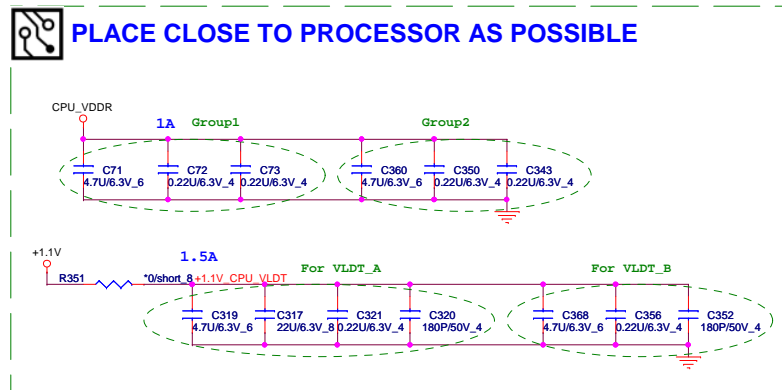
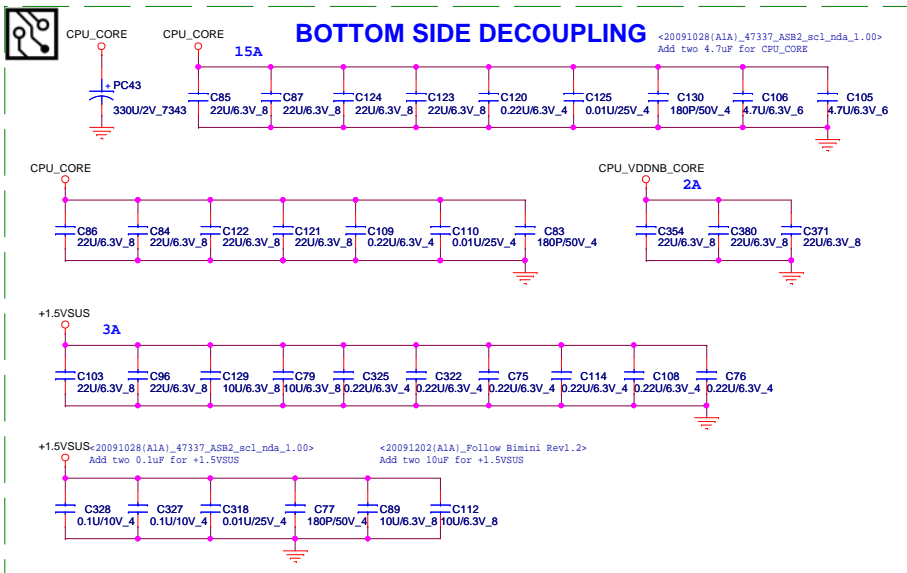
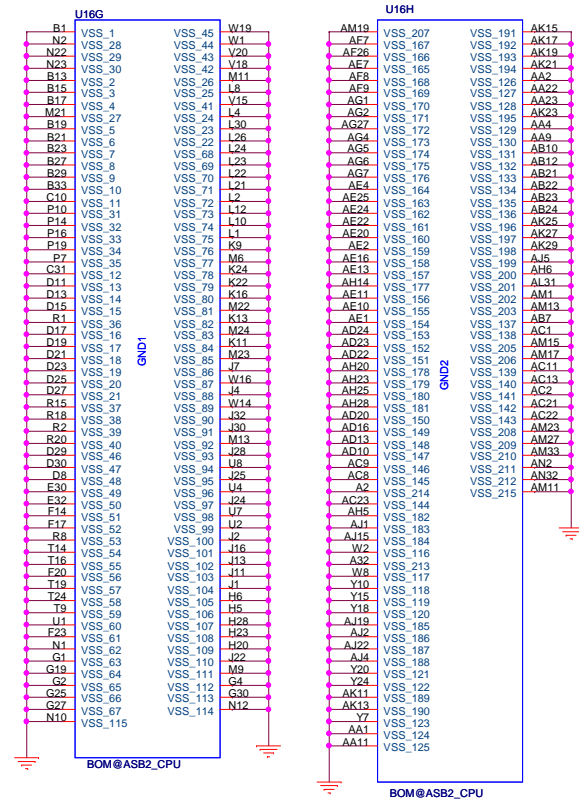
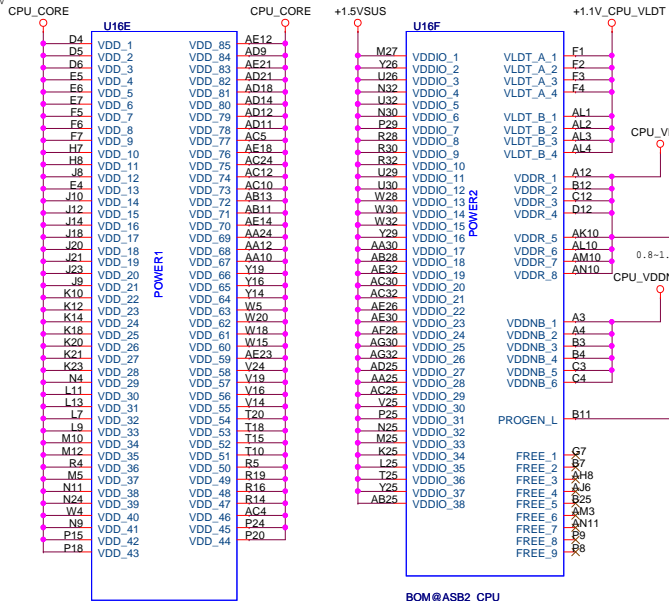
Size	Document Number	Rev
	ASB2 HT I/F 1/4	4A
Date:	Sunday, March 28, 2010	Sheet 2 of 40

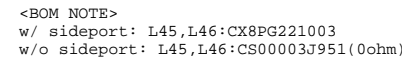
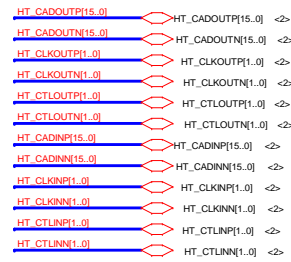
# Processor Memory Interface





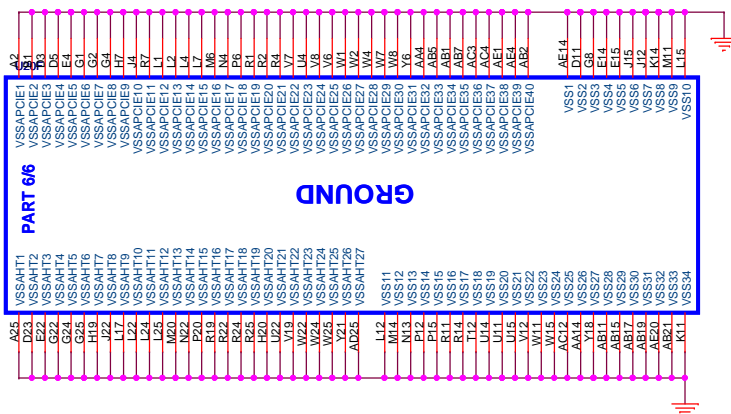
# PROCESSOR POWER AND GROUND





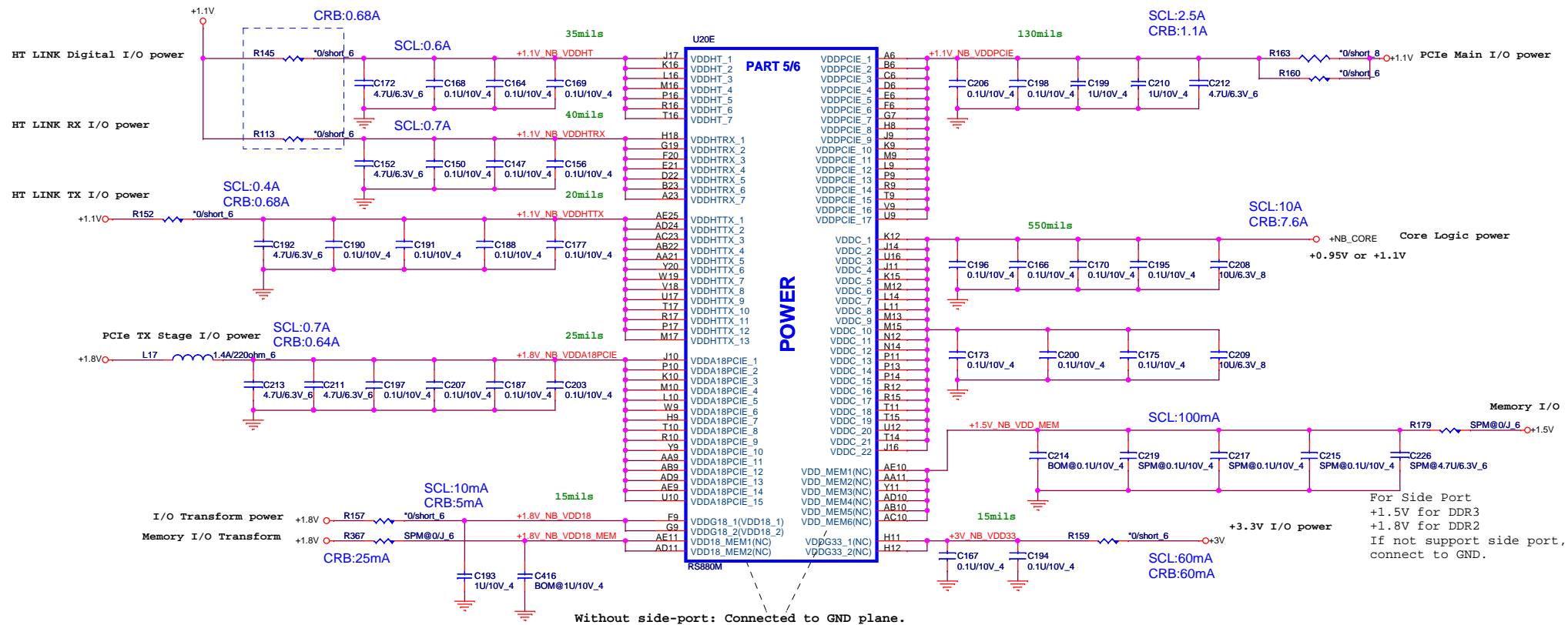






### RX881/RS880 POWER DIFFERENCE TABLE

PIN NAME	RX881	RS880	PIN NAME	RX881	RS880
VDDHT	+1.1V	+1.1V	IOPLLVD	+1.1V	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	GND	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	GND	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	GND	+1.8V
VDD18	+1.8V	+1.8V	PLLVD	GND	+1.1V
VDD18_MEM	GND	+1.8V	PLLVDH18	GND	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+0.95V~+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	GND	+1.8V/1.5V	VDDLTP18	GND	+1.8V
VDD33	+3.3V	+3.3V	VDDL18	GND	+1.8V
IOPLLVD18	+1.8V	+1.8V	VDDL1833	NC	NC



<BOM NOTE>

w/ sideport: C214:CH4102K1B03 ; C416:CH5102K9B06

w/o sideport: C214,C416:CS00002JB38(0ohm)

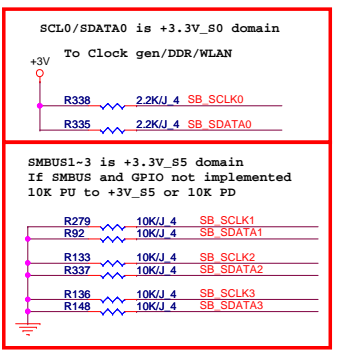
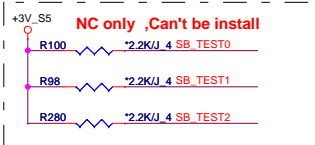


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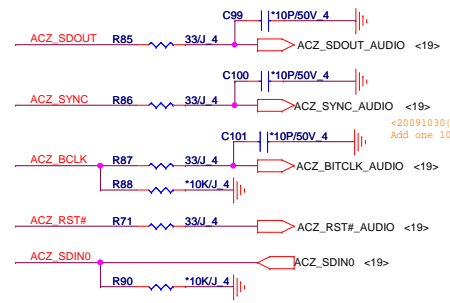
**PROJECT : ZH9**

Size	Document Number	Rev
	<b>RS880-POWER 4/4</b>	4A
Date:	Sunday, March 28, 2010	Sheet 9 of 40

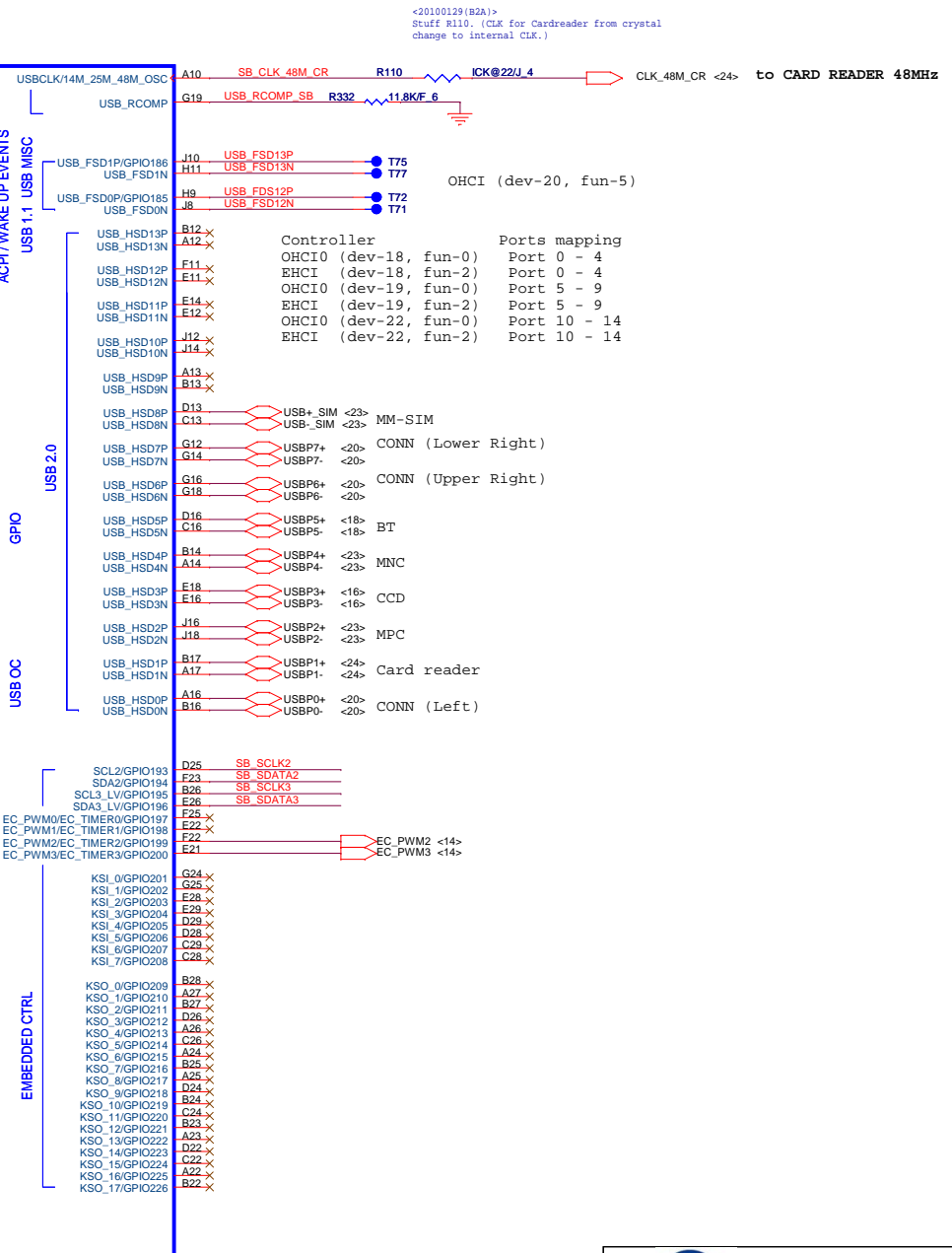
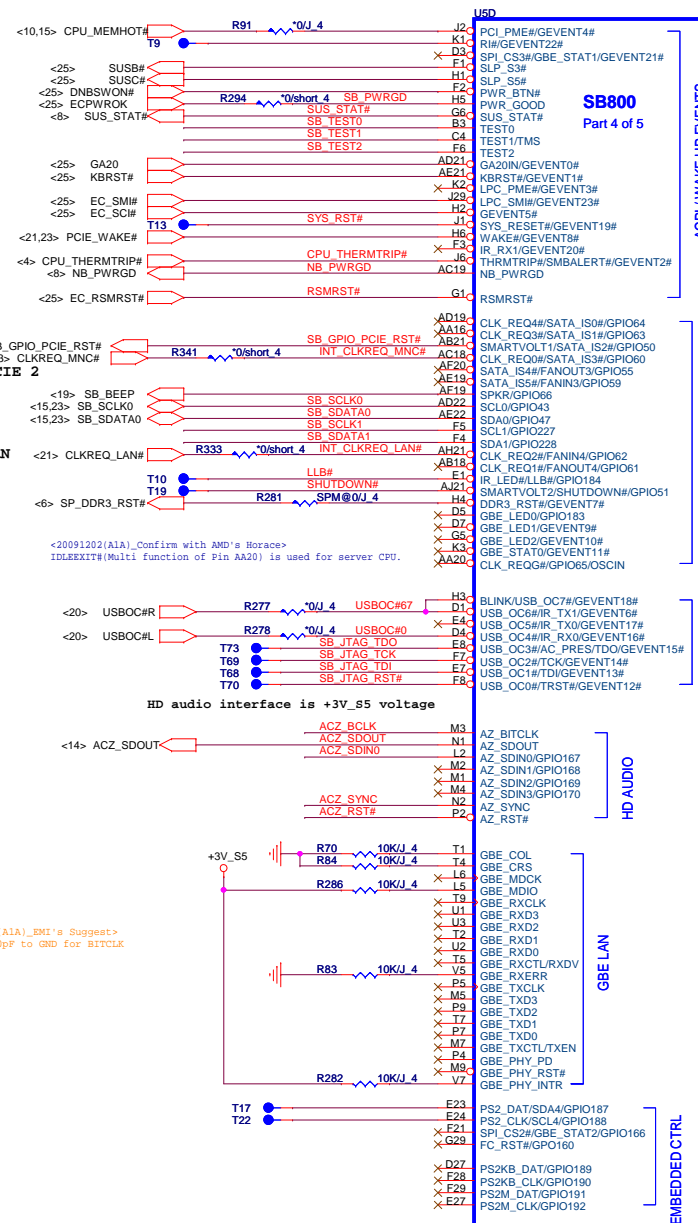




To Azalia



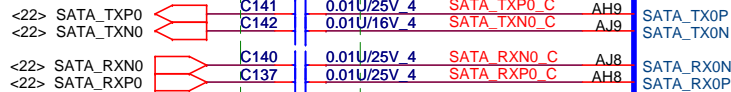
<20091030[ALA]\_EMI's Suggest>  
Add one 10pF to GND for BitCLK



SATA PORT 0,1,2,3  
can support AHCI  
mode

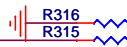
PLACE SATA AC COUPLING  
CAPS CLOSE TO SB820

SATA HDD

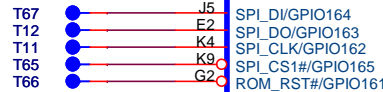
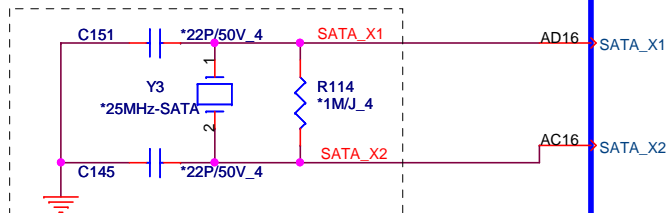
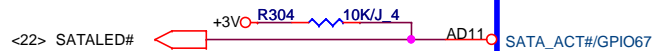


PLACE SATA\_CAL  
RES VERY CLOSE  
TO BALL OF SB820

+1.1V\_SB\_VDDAN\_11\_SATA



To meet SB800 SCL1.02:  
DNI SATA XTAL circuit's parts



SB800

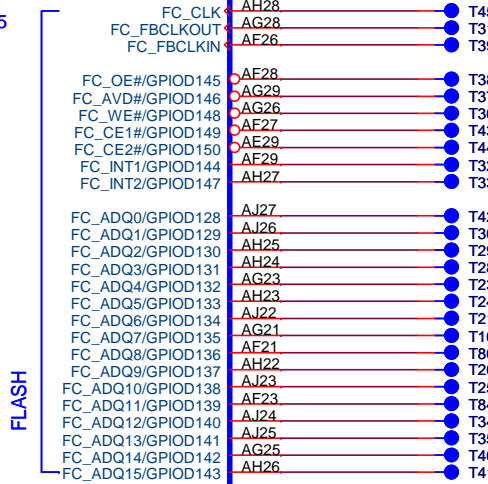
Part 2 of 5

SERIAL ATA

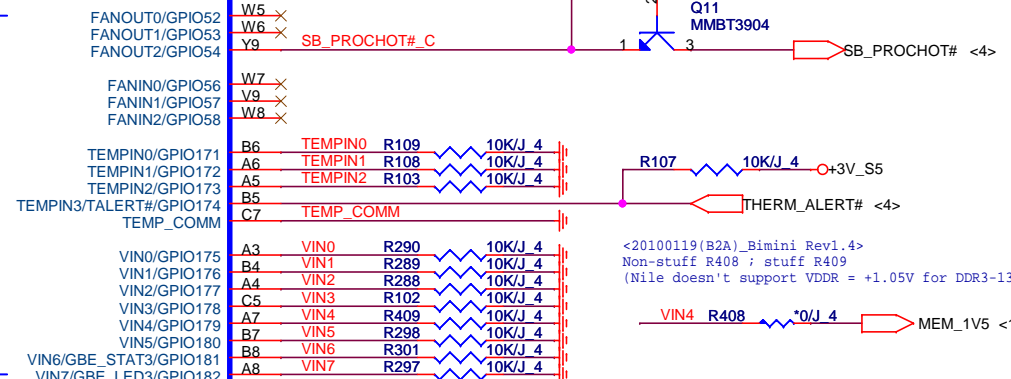
HW MONITOR

SPI ROM

The flash controller function is NOT  
supported by the SB820M.



IF THERE IS NO IDE, TEST  
POINTS FOR DEBUG BUS  
IS MANDATORY



<20100119(B2A)\_Bimini Rev1.4>  
Non-stuff R408 ; stuff R409  
(Nile doesn't support VDDR = +1.05V for DDR3-1333)

VIN4 R408 \*0/J\_4 MEM\_1V5 <10>



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PROJECT : ZH9

Size	Document Number	Rev
	SB820-SATA/HWM/SPI 3/5	4A
Date:	Sunday, March 28, 2010	Sheet 12 of 40

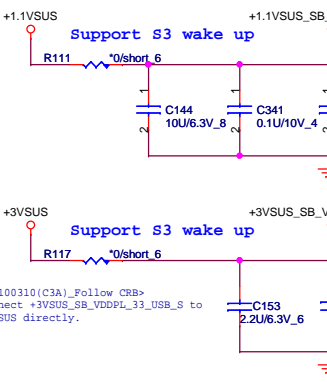
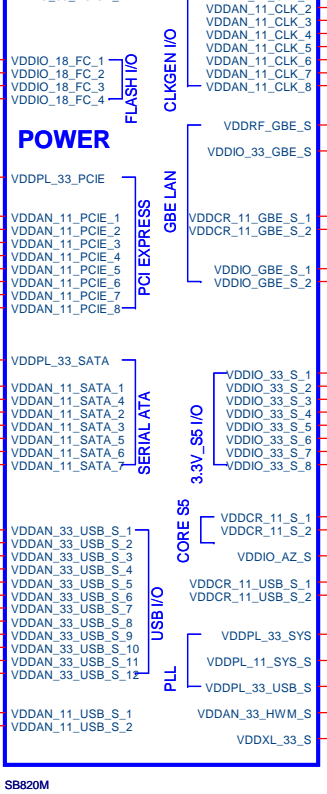
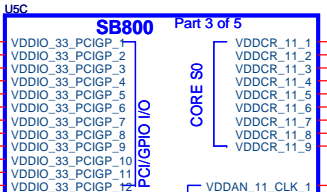
USC

**SB800** Part 3 of 5

VDDIO_33_PCI0P_1	CORE S0	VDDCR_11_1
VDDIO_33_PCI0P_2		VDDCR_11_2
VDDIO_33_PCI0P_3		VDDCR_11_3
VDDIO_33_PCI0P_4		VDDCR_11_4
VDDIO_33_PCI0P_5		VDDCR_11_5
VDDIO_33_PCI0P_6		VDDCR_11_6
VDDIO_33_PCI0P_7		VDDCR_11_7
VDDIO_33_PCI0P_8		VDDCR_11_8
VDDIO_33_PCI0P_9		VDDCR_11_9
VDDIO_33_PCI0P_10		
VDDIO_33_PCI0P_11		
VDDIO_33_PCI0P_12		

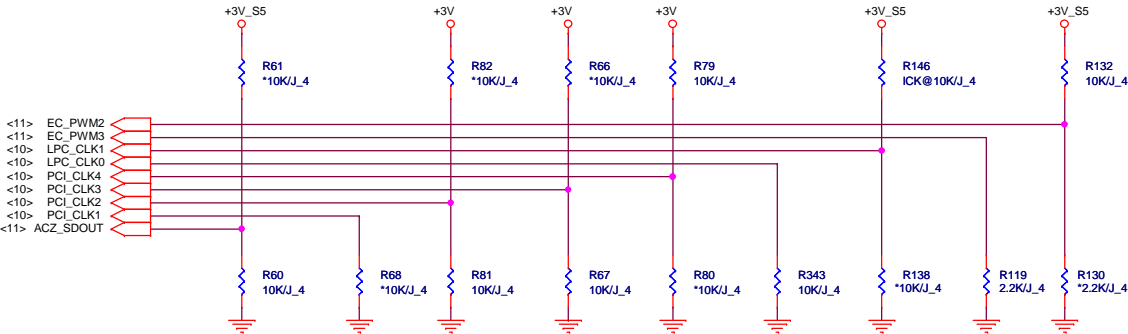
PCI/GPIO I/O

VDDAN 11 CLK 1



STANDARD STRAPS

<20091202(A1A)\_Confirm with AMD's Horace>  
PCI\_CLK4 PU with 10K for both internal and external CLK Gen.



	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM3	EC_PWM2
PULL HIGH	LOW POWER MODE	PCIe Gen II	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLK MODE ICK@DEFAULT	EC ENABLED	CLKGEN ENABLED ICK@DEFAULT	H, H=Reserved H, L=SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	PCIe Gen I	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	FUSION CLK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED ECK@DEFAULT	L, H=LPC ROM L, L=Reserved	DEFAULT

This is required as the low power mode is not supported on the SB8xx.

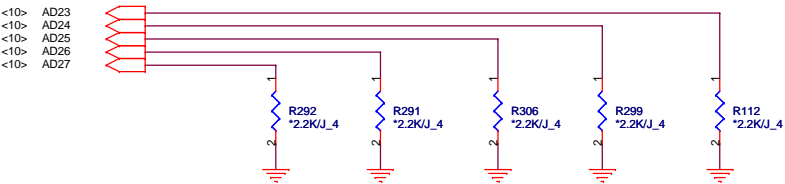
Not Applicable to SB820M--Leave provision for PD.

PCICLK4: CPU/NB HT Clock Selection  
This strap is not used if the strap CLKGEN is configured for external clock generator mode.


internal have pull Hi 10K

DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI\_AD[27:23]



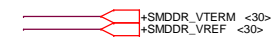
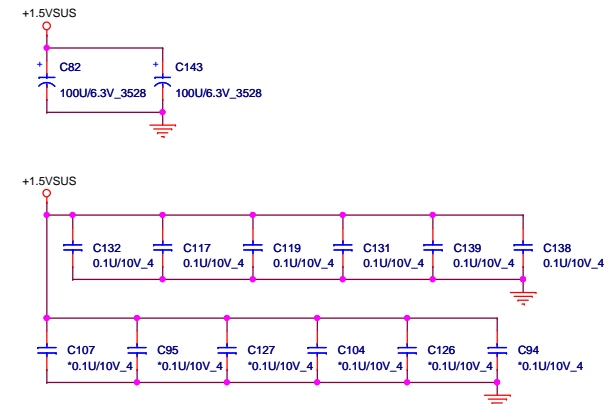
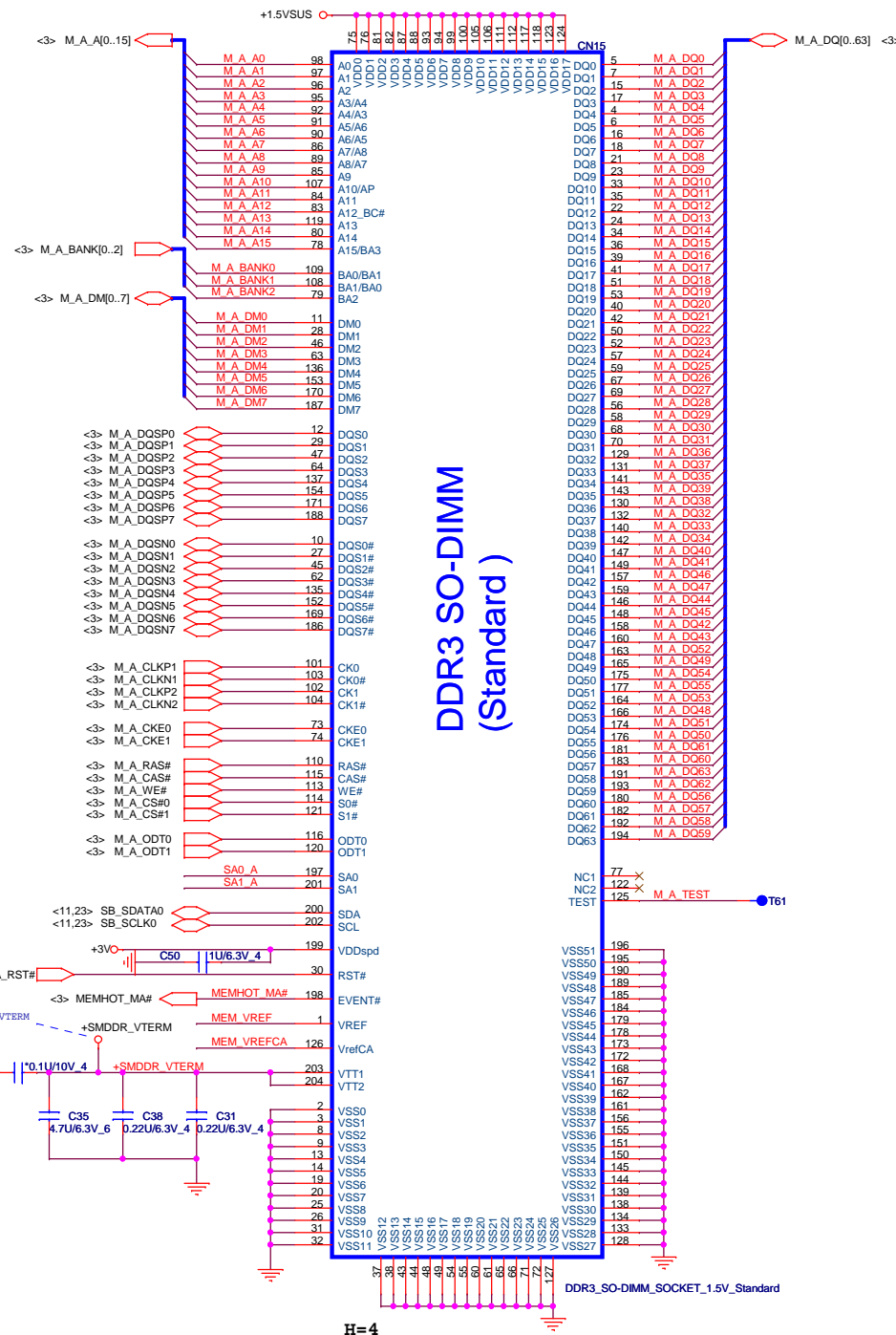
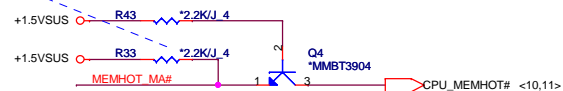
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



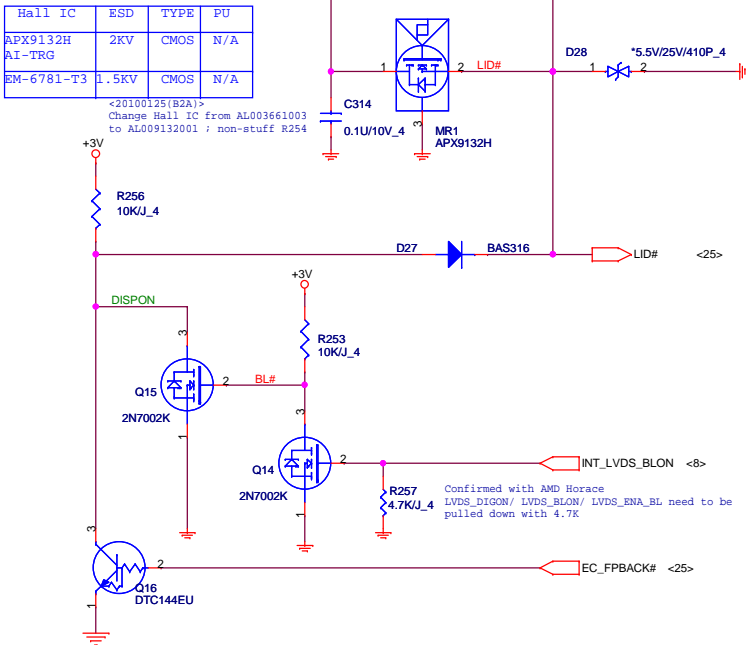
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PROJECT : ZH9

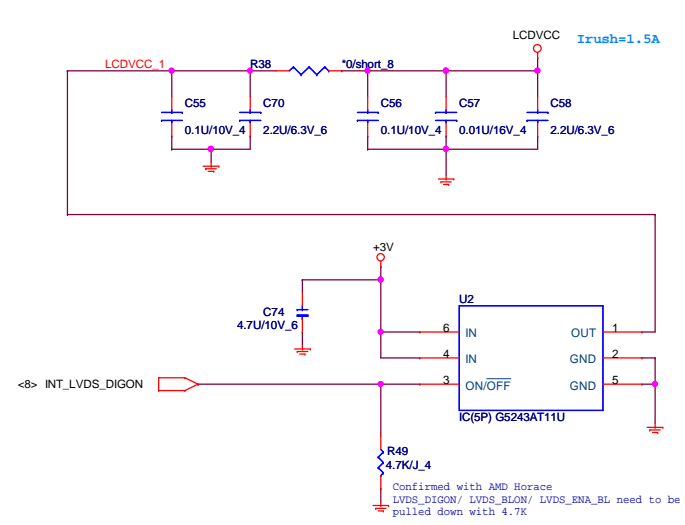
Size	Document Number	Rev
	SB820-STRAPS,PWRGD 5/5	4A
Date:	Sunday, March 28, 2010	Sheet 14 of 40



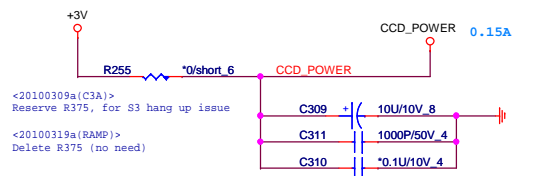
HALL IC(HSR)



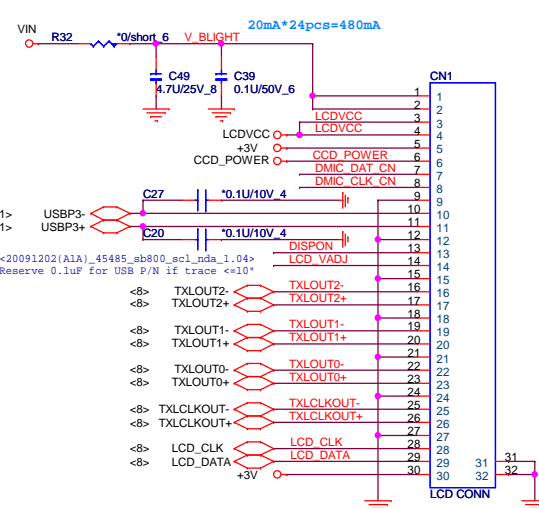
LCD POWER SWITCH(LDS)



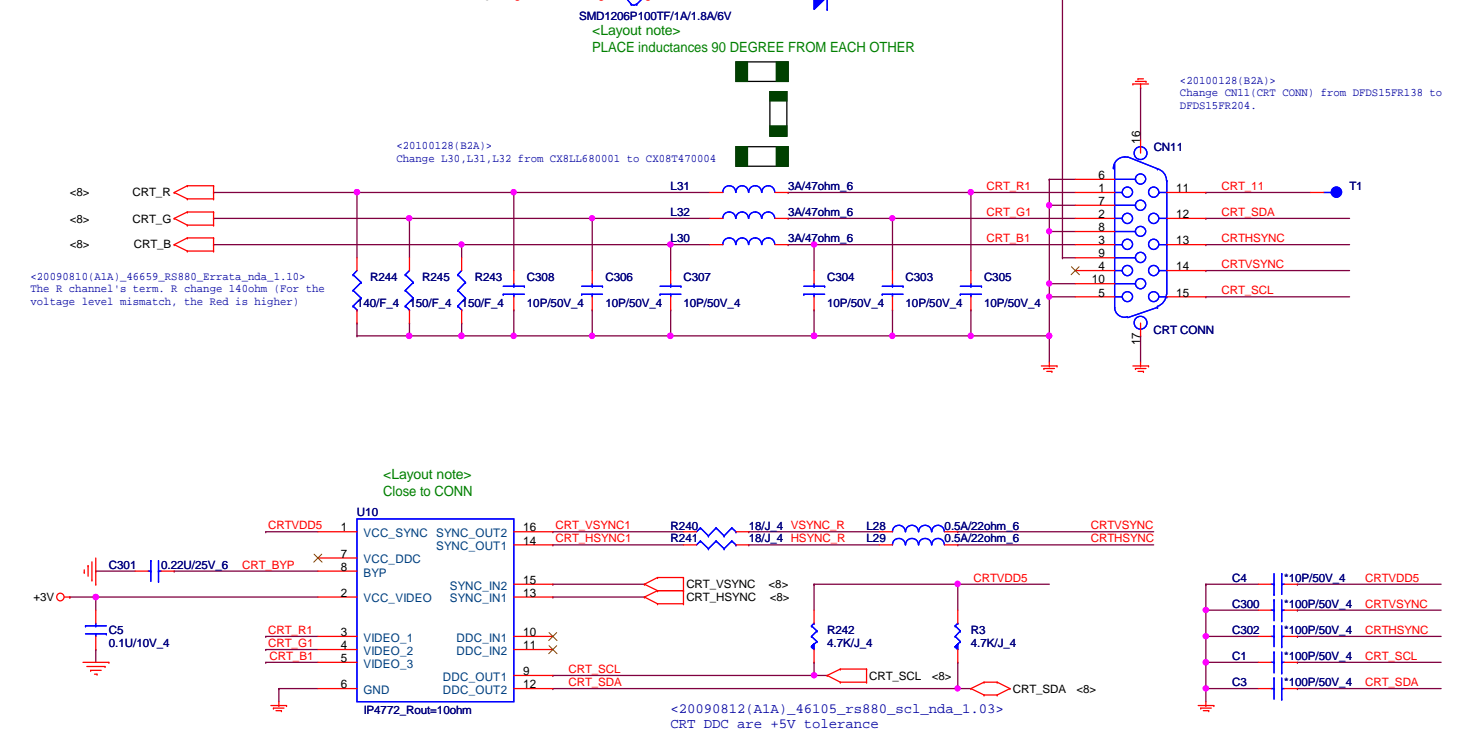
CAMERA POWER(CCD)



LCD MODULE(LDS)

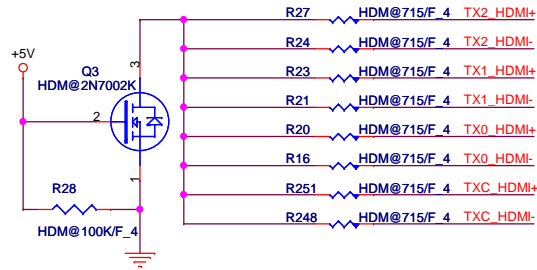


CRT(CRT)



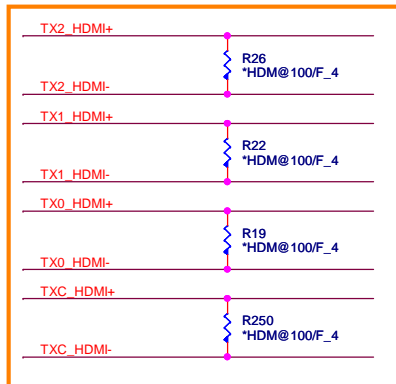
## (HDM)

### Close to HDMI Connector



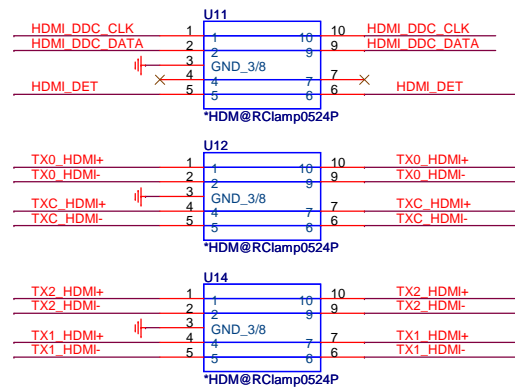
## EMI reserve for HDMI(HDM)

Close connector

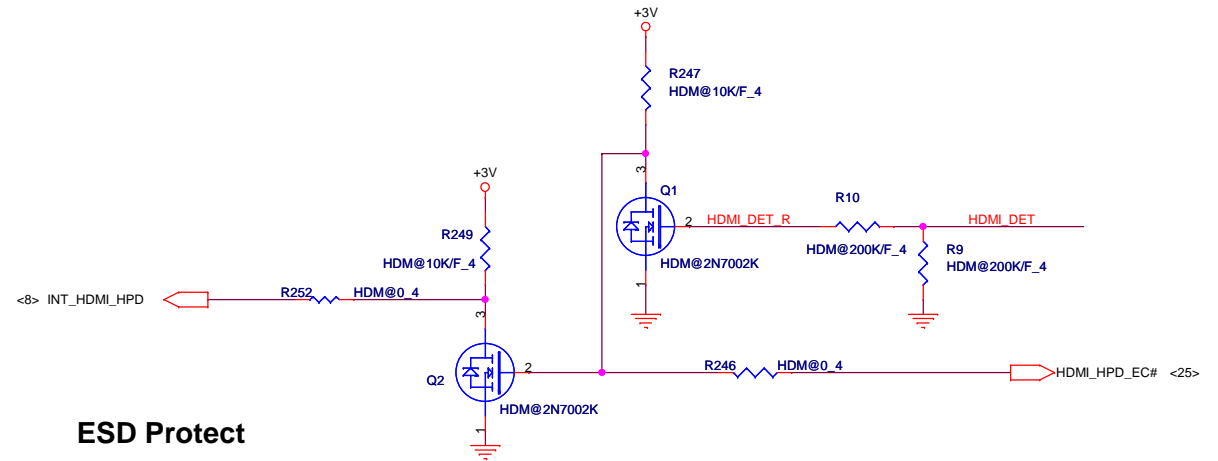


## ESD Protect

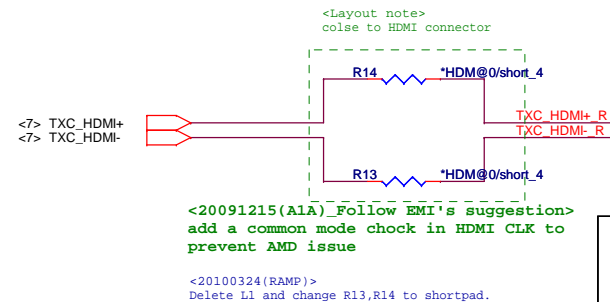
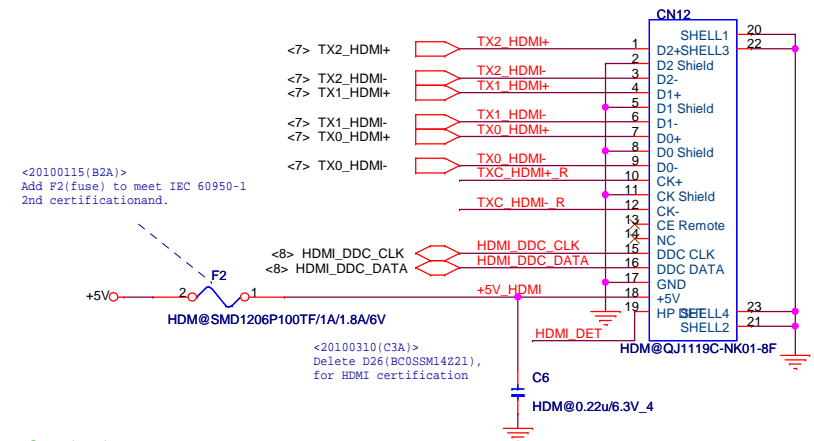
close to HDMI connector



## HDMI HPD SENSE

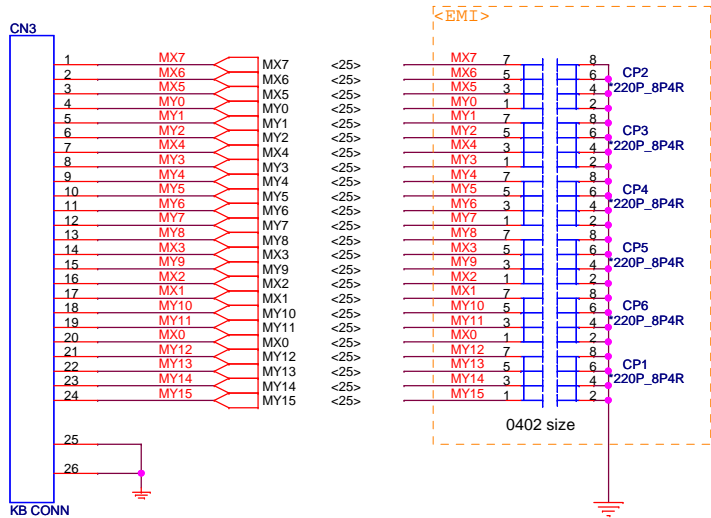


## HDMI PORT



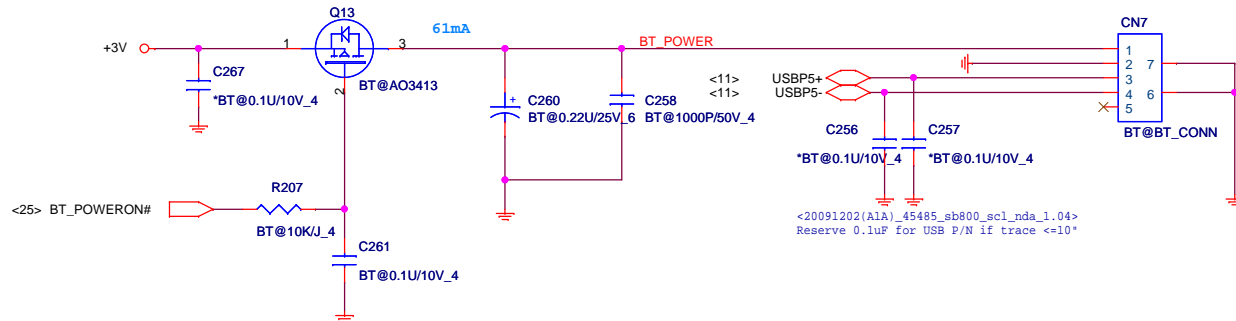
## KEYBOARD(KBC)

```
<20100303(C3A)>
Change CP1-CP6 footprint from 8p4r-0402 to
8p4r-0402-smt, for SMT open issue.
```

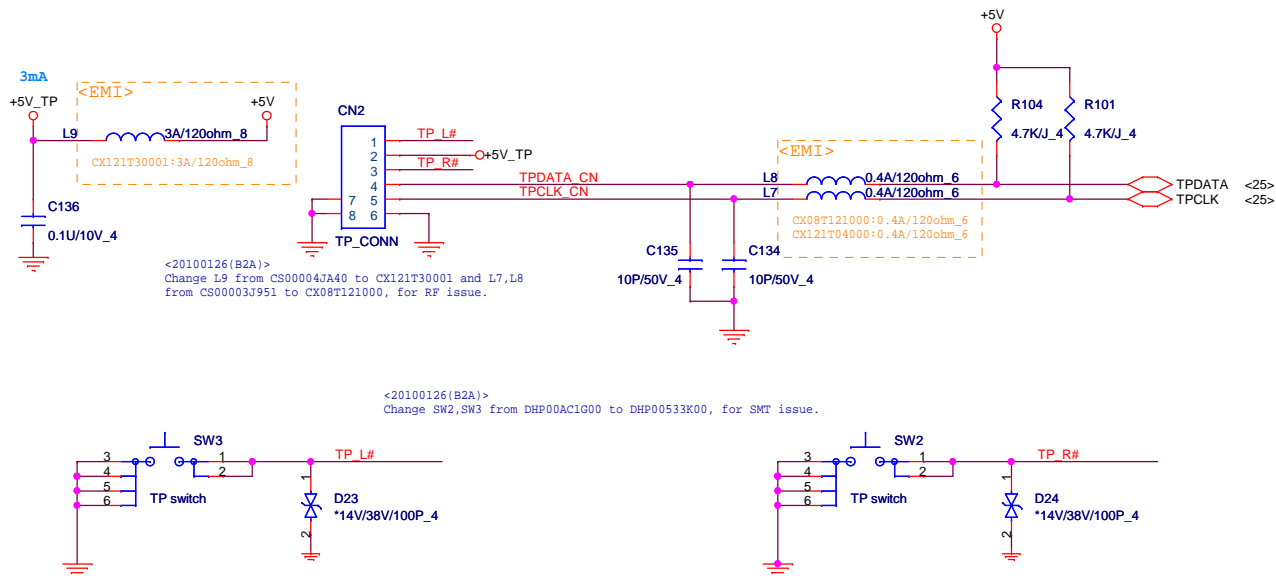


## BLUETOOTH(BTM)

BT	PWR	LED
T77H056.00	+3V	
T60H928.33	+3V	



## TOUCH PAD(TPD)

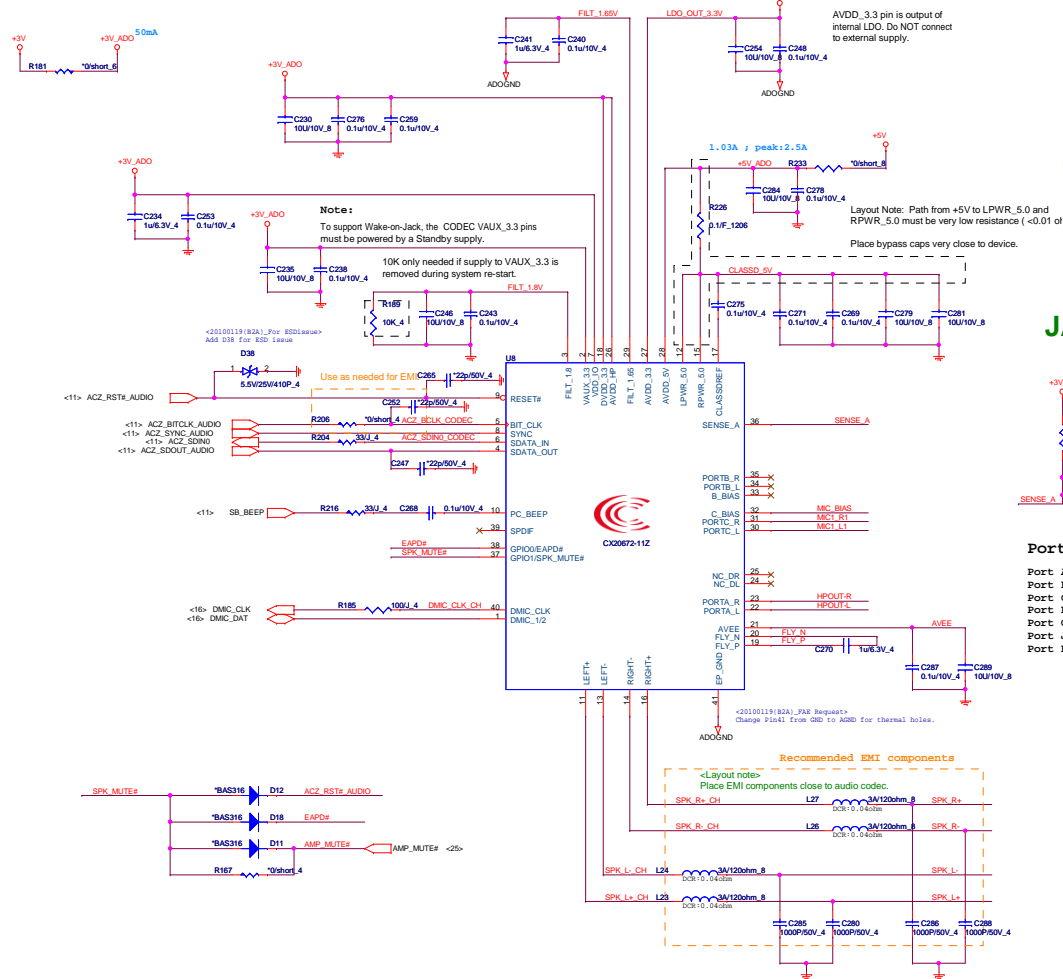


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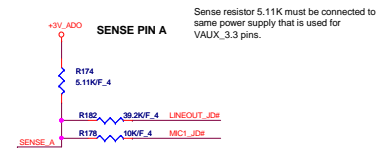
**PROJECT : ZH9**

Size	Document Number	Rev
	<b>KB/BT/TP/LED/Power Connector</b>	4A
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## AUDIO CODEC

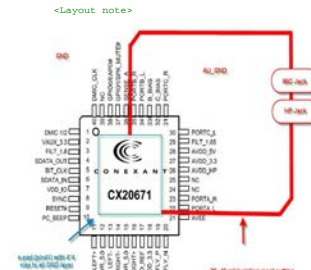
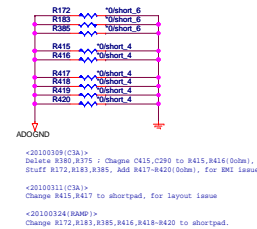


## JACK DETECT RESISTORS

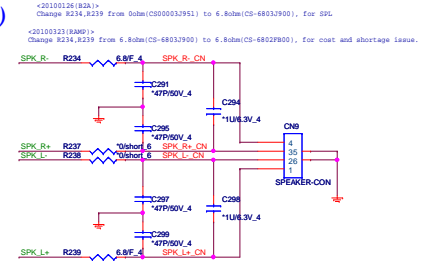


## Port Configuration

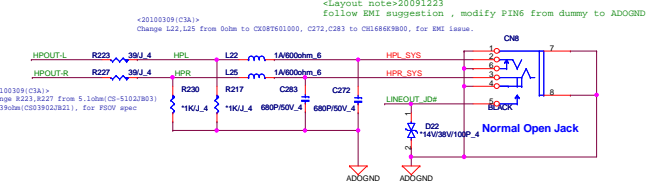
Port A: Headphone jack (jack shared with S/PDIF)  
Port B: Internal analog mono mic (stereo option)/Line In  
Port C: Microphone jack  
Port D: LineOut jack(need cap) or Headphone jack(cap less)  
Port G: Internal stereo speakers  
Port J: Optional Internal stereo digital mic  
Port H: S/PDIF (jack shared with headphone)



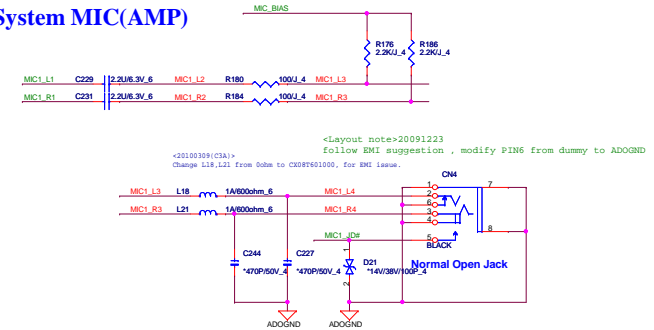
*Speaker (AMP)*



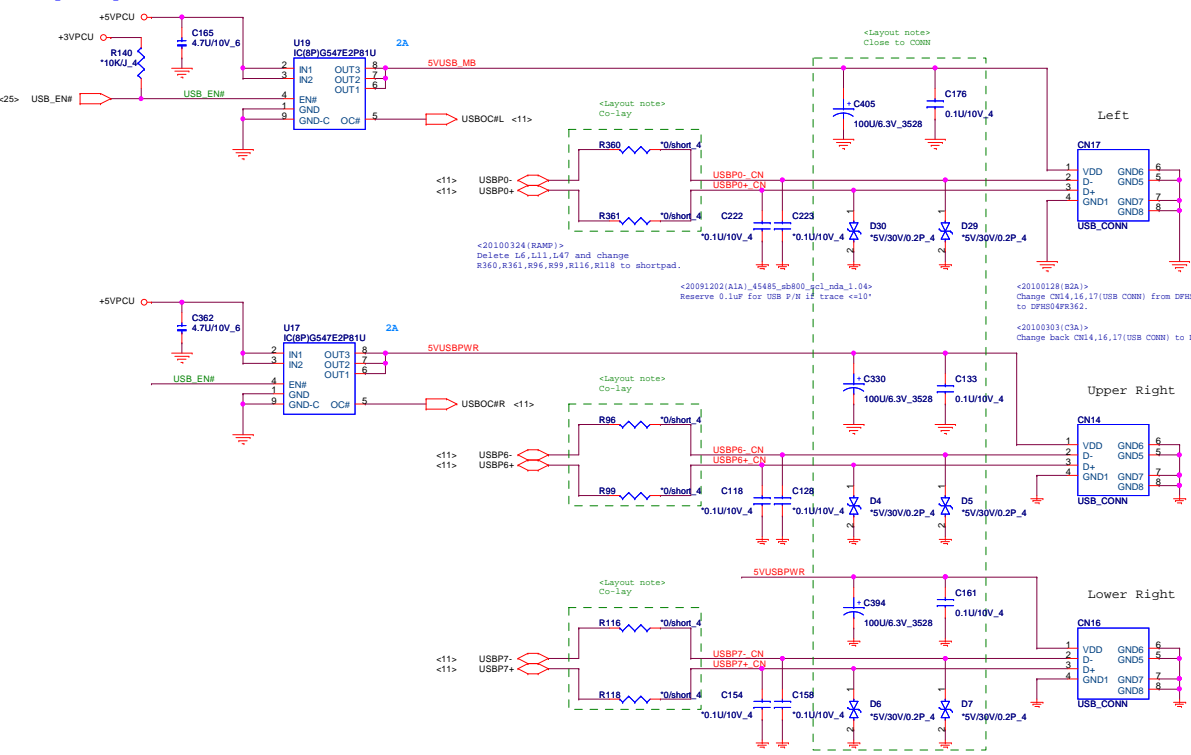
### Earphone(AMP)



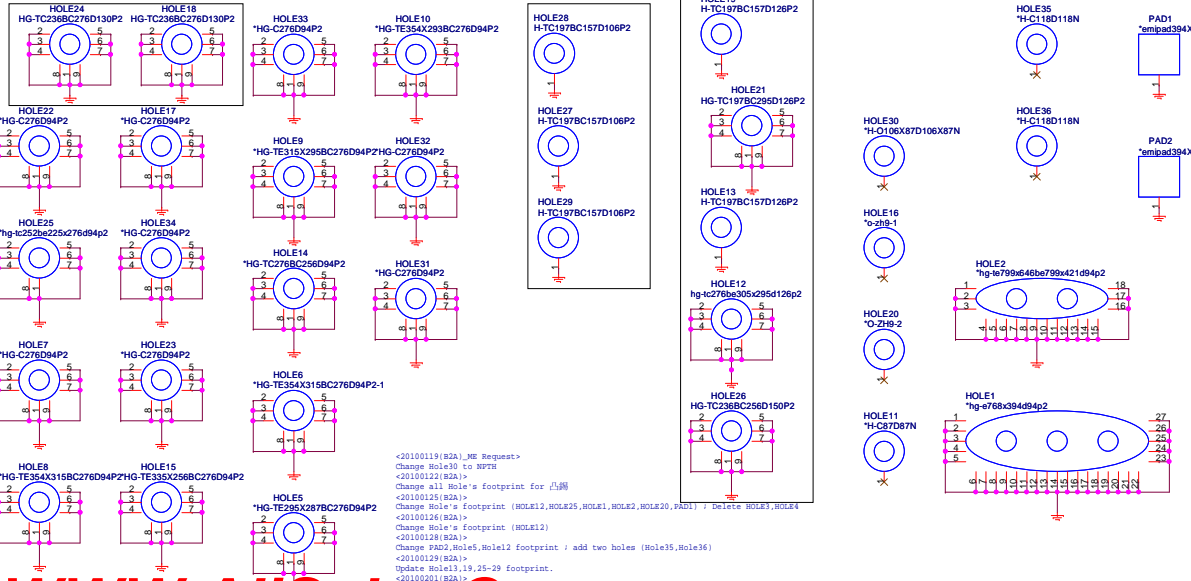
## System MIC(AMP)



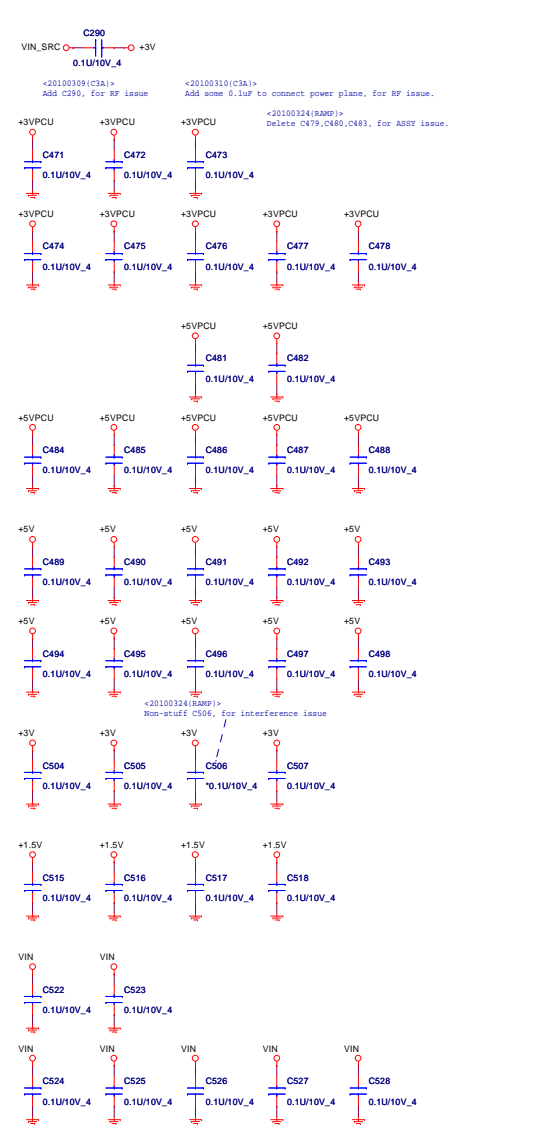
USB(USB)



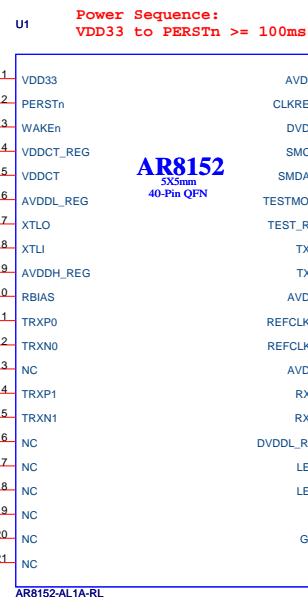
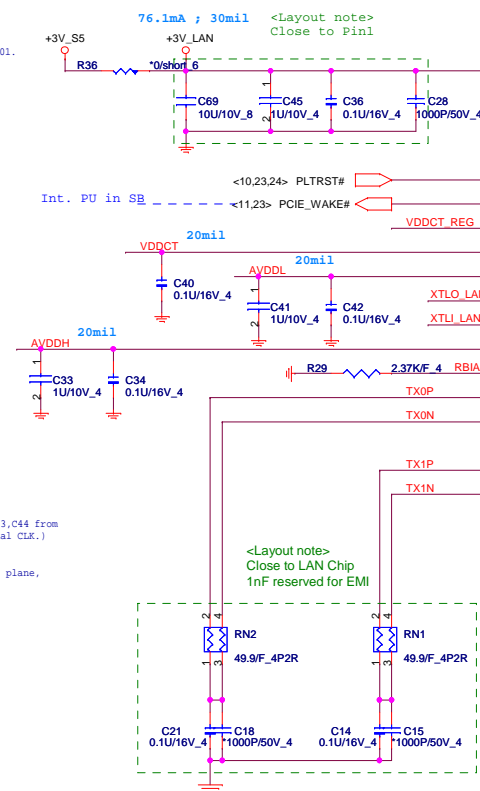
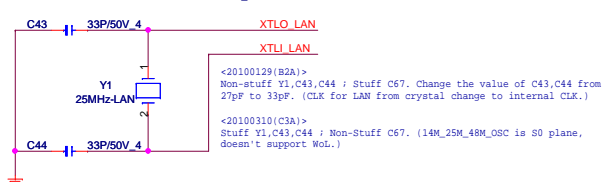
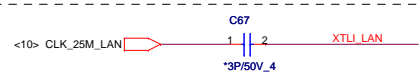
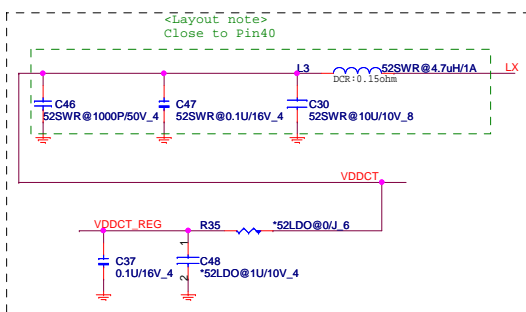
HOLE(OTH)



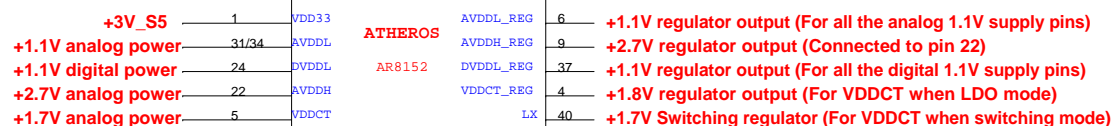
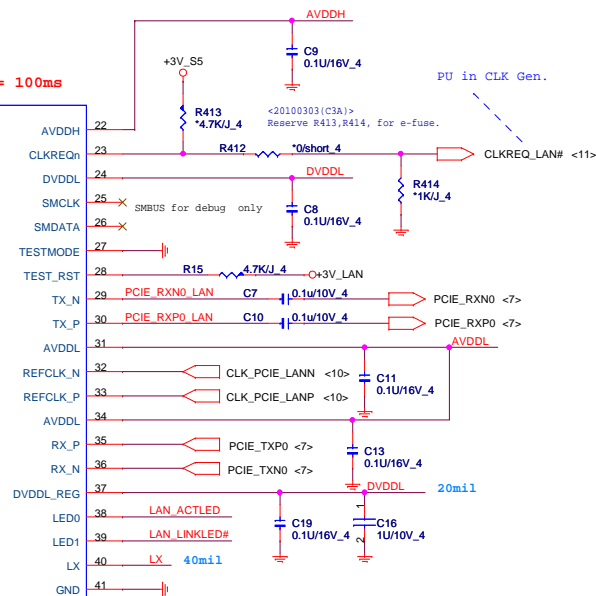
EMI (EMC)



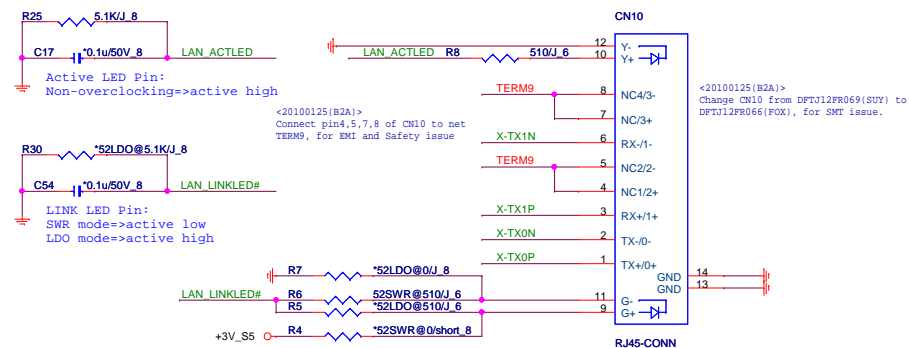
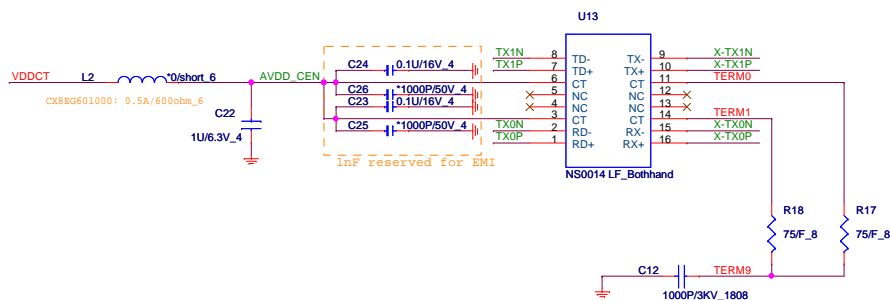
5	4
<pre> &lt;BOM note&gt; If center tap power come from internal switch regulator =&gt;Stuiff 52SWR@ (Default) If center tap power come from internal LDO =&gt;Stuiff 52LDO@                                 &lt;20100303(C3A)_FAE's suggestion&gt;                                 Change L3 from CV-4710N03 to CV-4710T201. </pre>	



AR8152-A : w/o 802.3az  
AR8152-B : w/ 802.3az



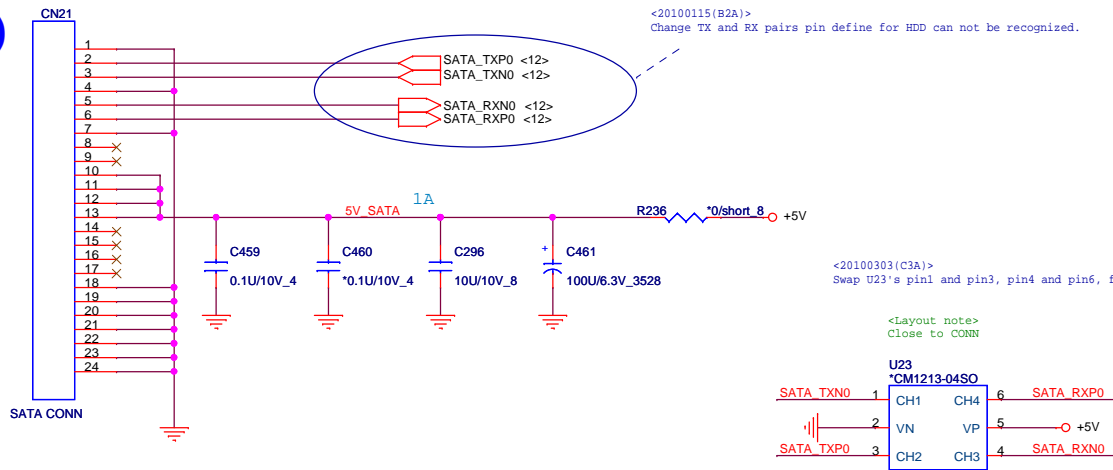
# TRANSFORMER

**Quanta Computer Inc.**

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Size	Document Number <b>LAN AR8152L</b>	Rev 4A
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## 2.5" SATA HDD(HDD)

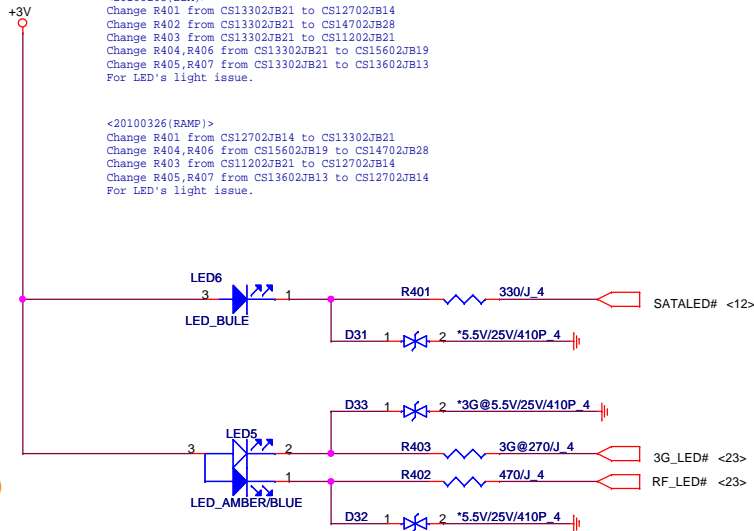


## LED/SW(UIF)

<20091214(A1A)\_Confirm with Acer Johnson\_Yeh>  
The JV01\_NL and SJV01\_NL had 4 LEDs --> Power / Battery / HDD / Communication

<20100203(B2A)>  
Change R401 from CS13302JB21 to CS12702JB14  
Change R402 from CS13302JB21 to CS14702JB28  
Change R403 from CS13302JB21 to CS11202JB21  
Change R404, R406 from CS13302JB21 to CS15602JB19  
Change R405, R407 from CS13302JB21 to CS13602JB13  
For LED's light issue.

<20100326(RAMP)>  
Change R401 from CS12702JB14 to CS13302JB21  
Change R404, R406 from CS15602JB19 to CS14702JB28  
Change R403 from CS11202JB21 to CS12702JB14  
Change R405, R407 from CS13602JB13 to CS12702JB14  
For LED's light issue.



ID(Left-->Right)

Power LED/BATT LED/HDD LED/WiFi LED

<LED spec>

BLUE :

Vf = 2.7~3.2V ; If = 5mA

BLUE/ORANGE :

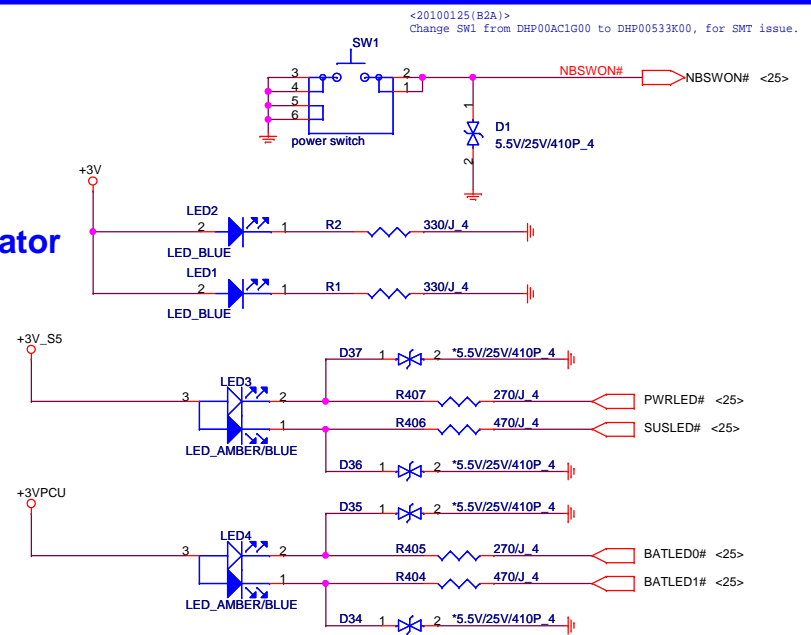
BH-Vf = 2.7~3.7V ; If = 20mA max=25mA

S2-Vf = 1.7~2.4V ; If = 20mA max=25mA

## PWR indicator

## PWR LED SUS LED

## FULL LED CHG LED

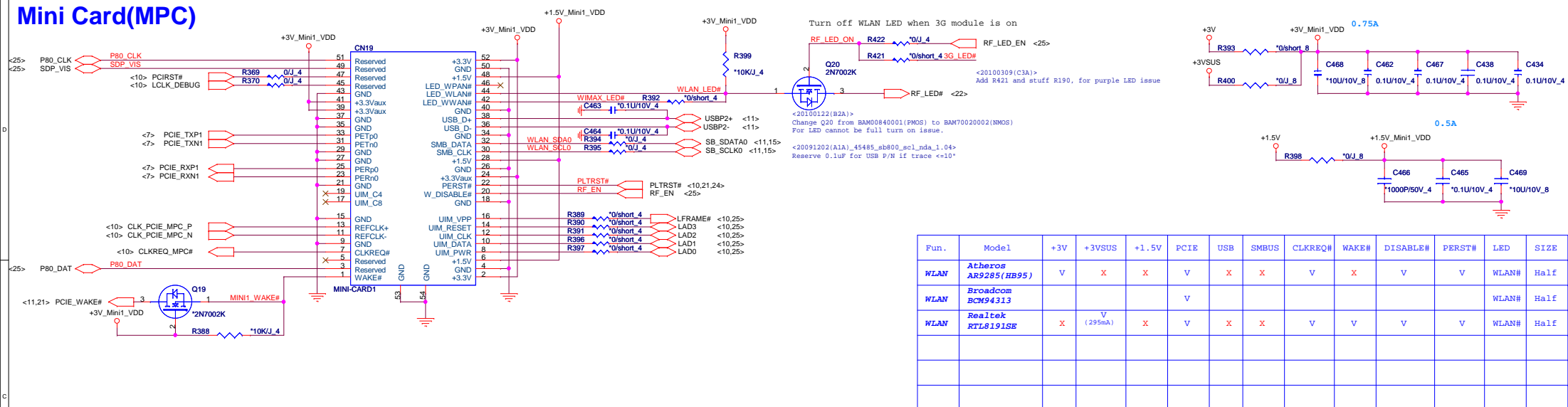


Quanta Computer Inc.

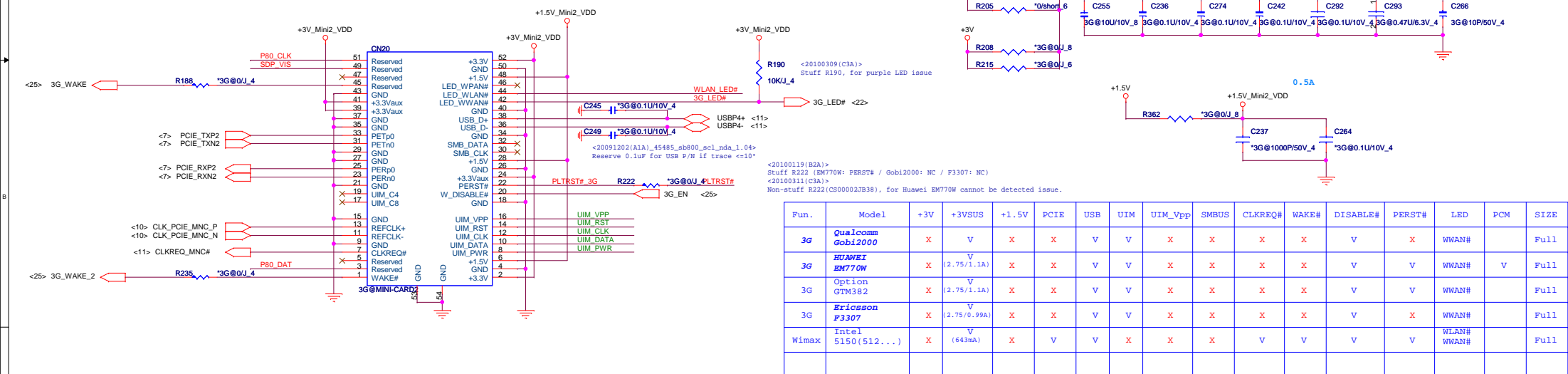
PROJECT : ZH9

Size	Document Number	Rev
	SATA HDD/LED/SW	4A
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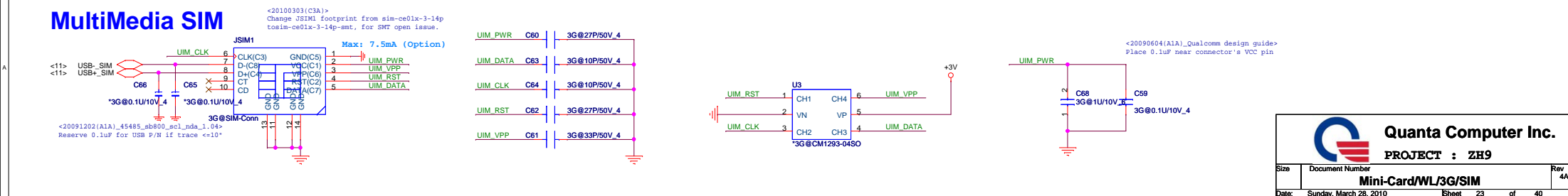
### Mini Card(MPC)



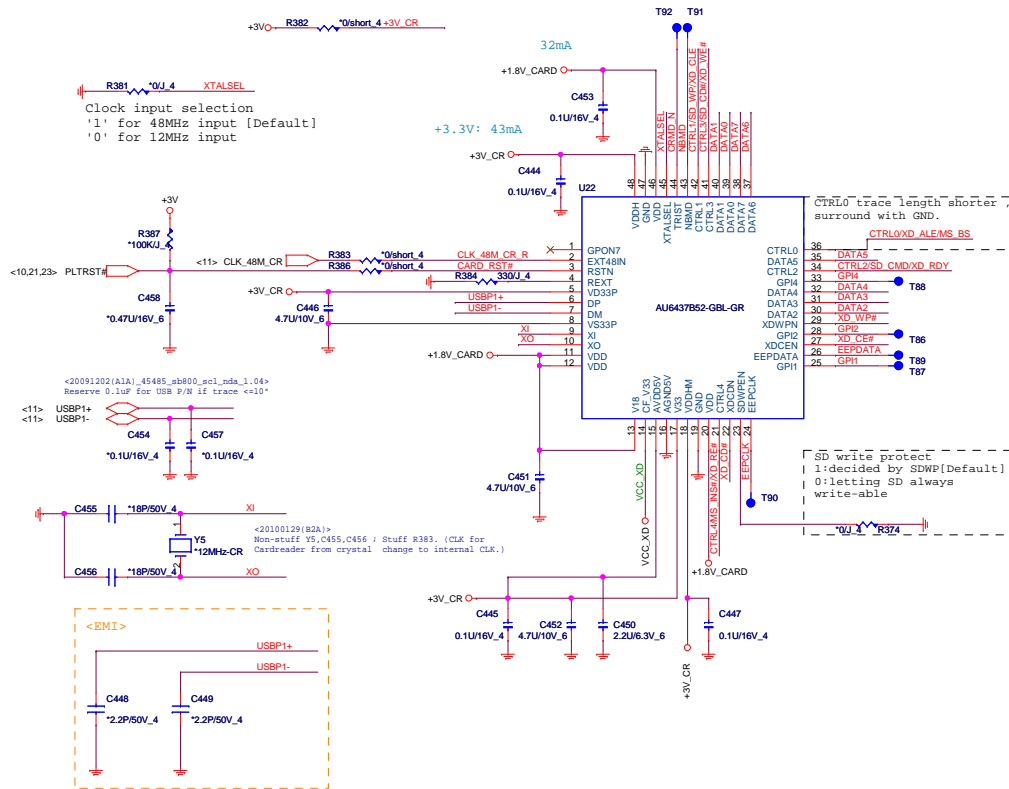
## Mini Card 2(MNC)



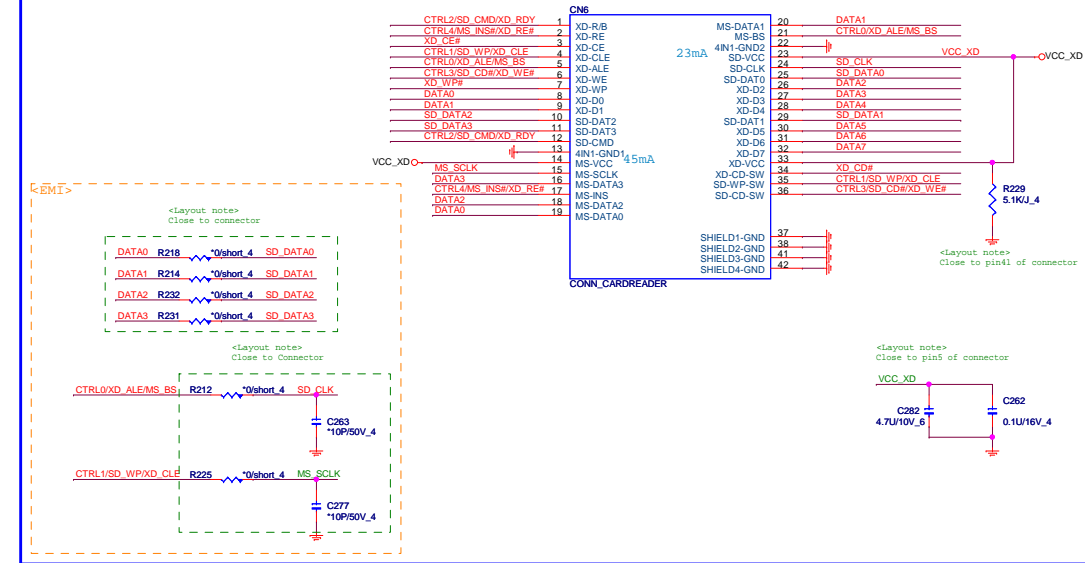
## MultiMedia SIM




## AU6437B52-GBL-GR (MMC)

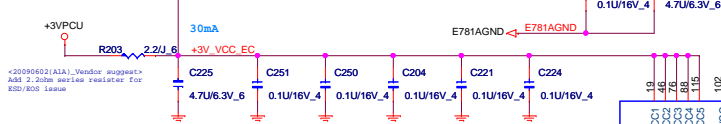


#### 4 IN 1 CARD READER (MMC)



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AU6437 (Card Reader)		
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# EC(KBC)



<Layout note>  
Place every 0.1uF  
close to every  
power pin

U6

A/D

D/A

LPC

GPIO

KB

TIMER

SPI

IR

SMB

PS/2

FIU

GPIO

GPIO

GPIO

GPIO

GPIO

GPIO

GPIO

A/D

D/A

LPC

GPIO

KB

TIMER

SPI

IR

SMB

PS/2

FIU

GPIO

GPIO

GPIO

GPIO

GPIO

GPIO

GPIO

A/D

D/A

LPC

GPIO

KB

TIMER

SPI

IR

SMB

PS/2

FIU

GPIO

GPIO

GPIO

GPIO

GPIO

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A/D

D/A

LPC

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KB

TIMER

SPI

IR

SMB

PS/2

FIU

GPIO

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A/D

D/A

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TIMER

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D/A

LPC

GPIO

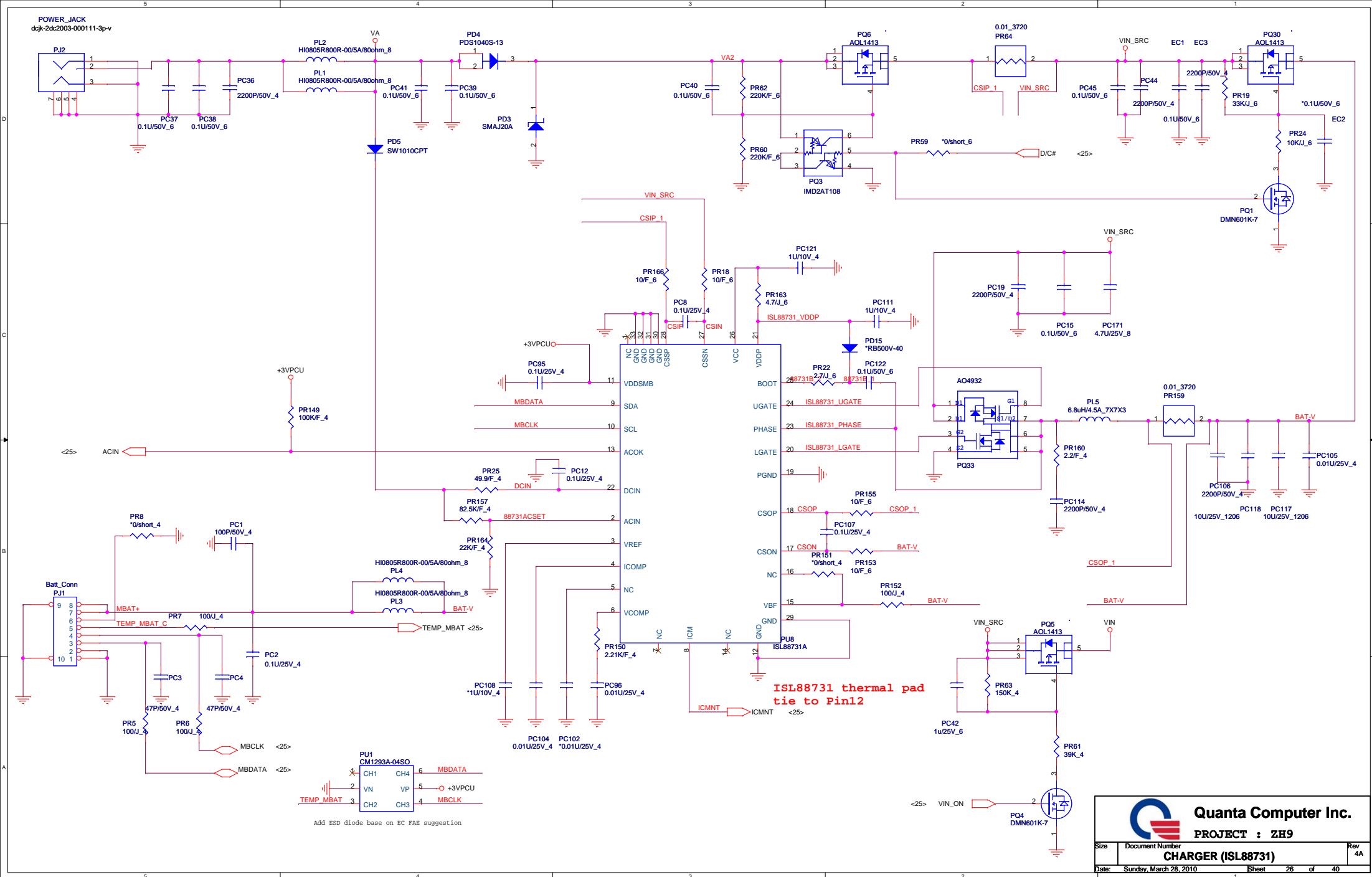
KB

TIMER

SPI

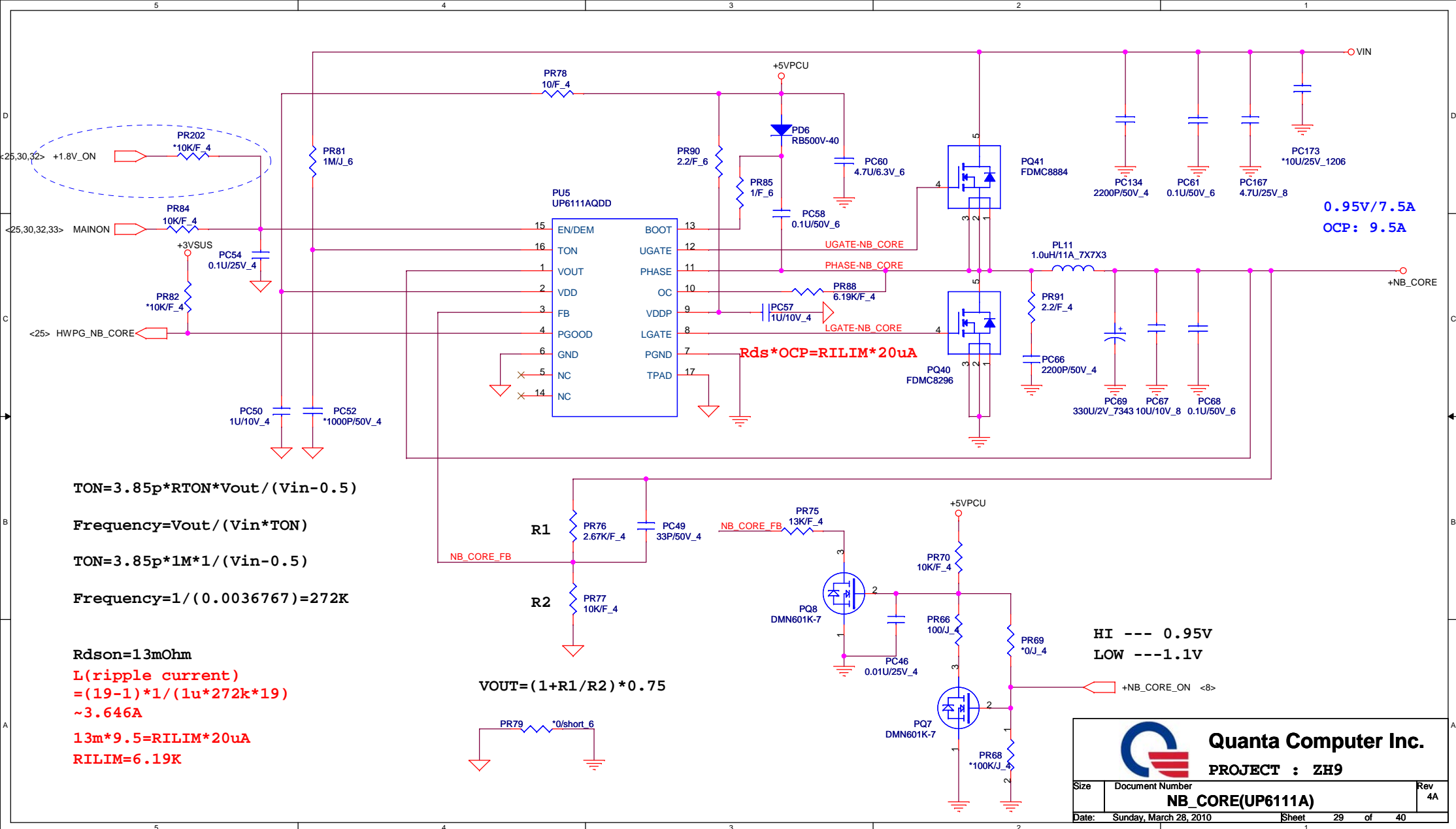
IR

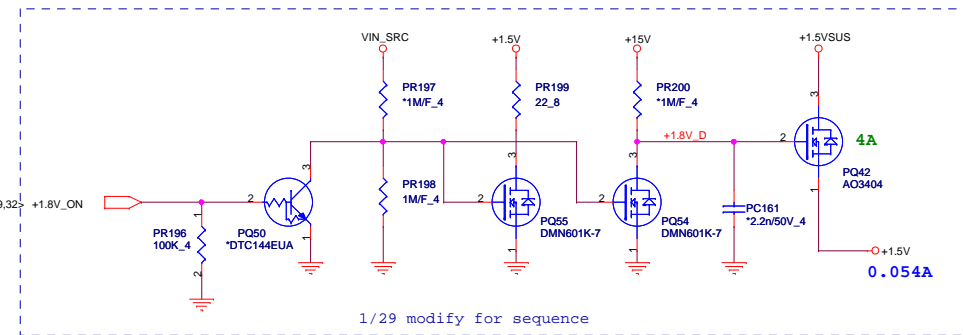
SMB

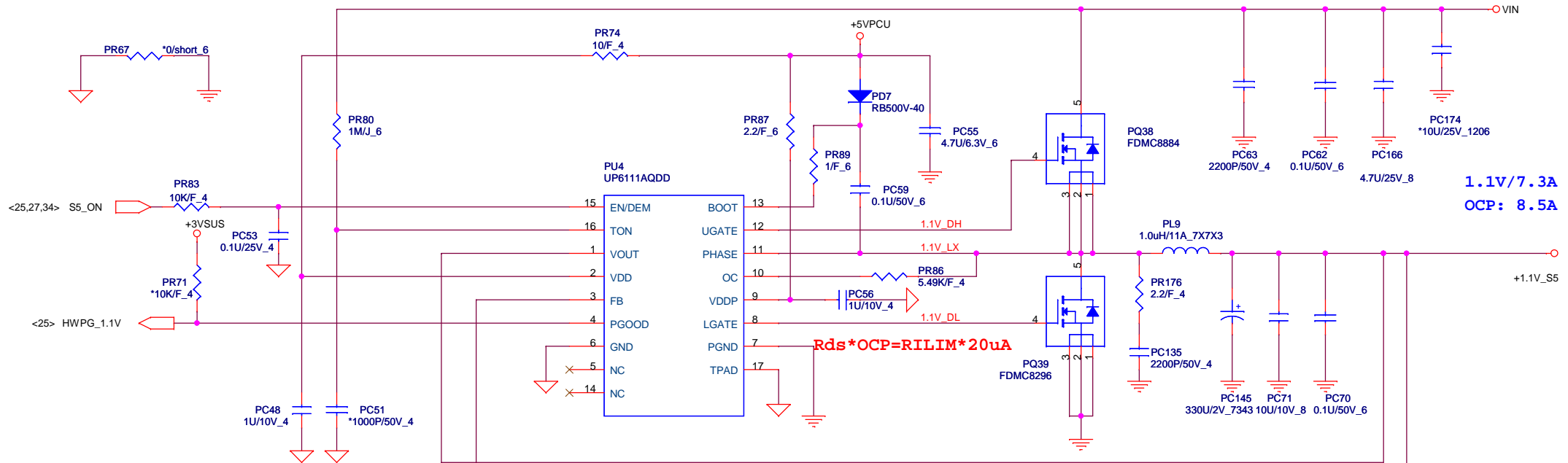












1.1V/7.3A  
OCP: 8.5A

$$V_{OUT} = (1 + R1/R2) * 0.75$$

$$T_{ON} = 3.85p * R_{TON} * V_{out} / (V_{in} - 0.5)$$

$$Frequency = V_{out} / (V_{in} * T_{ON})$$

$$T_{ON} = 3.85p * 1M * 1 / (V_{in} - 0.5)$$


$$Frequency = 1 / (0.0036767) = 272K$$

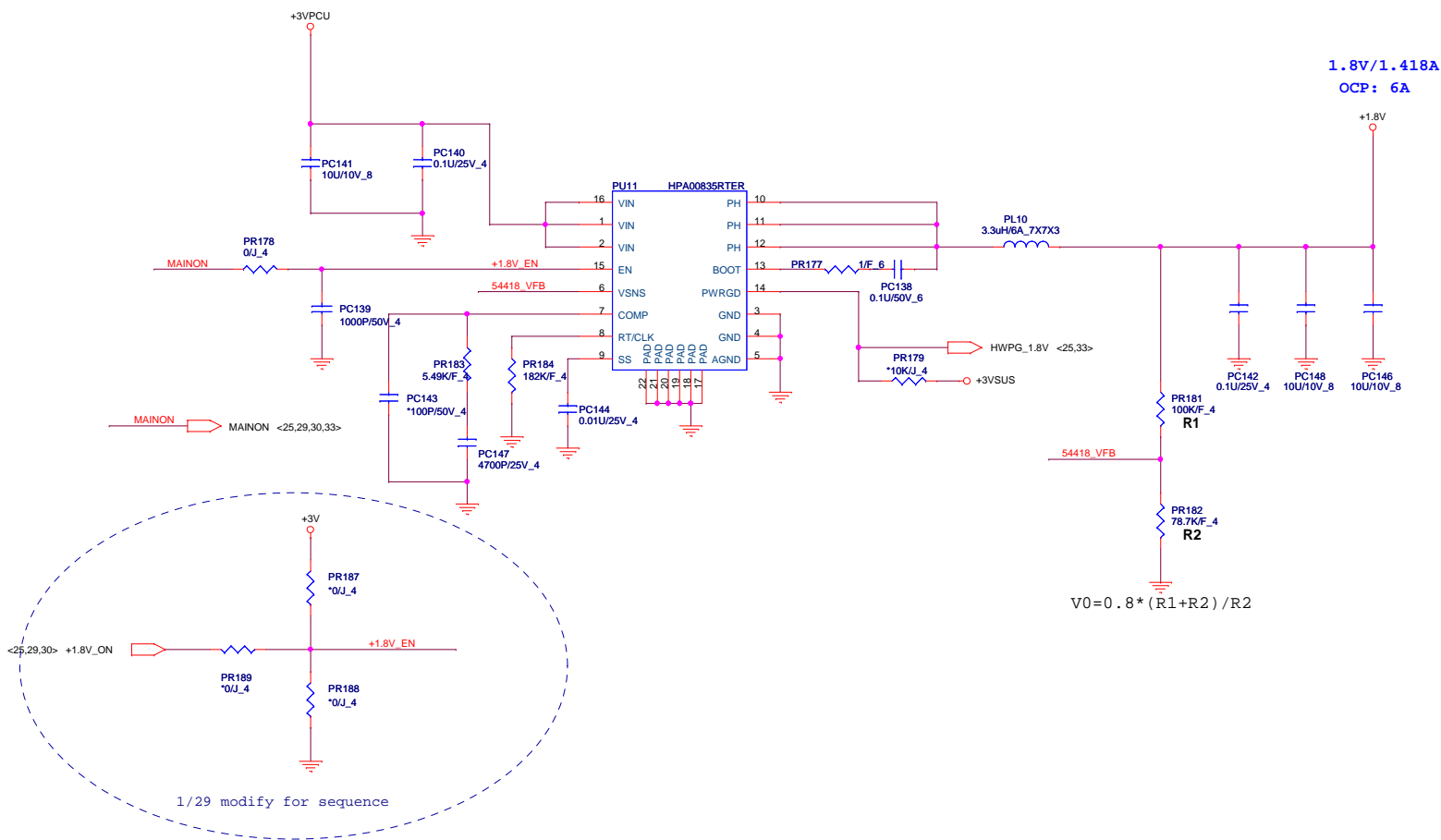
$$R_{dson} = 13m\Omega$$

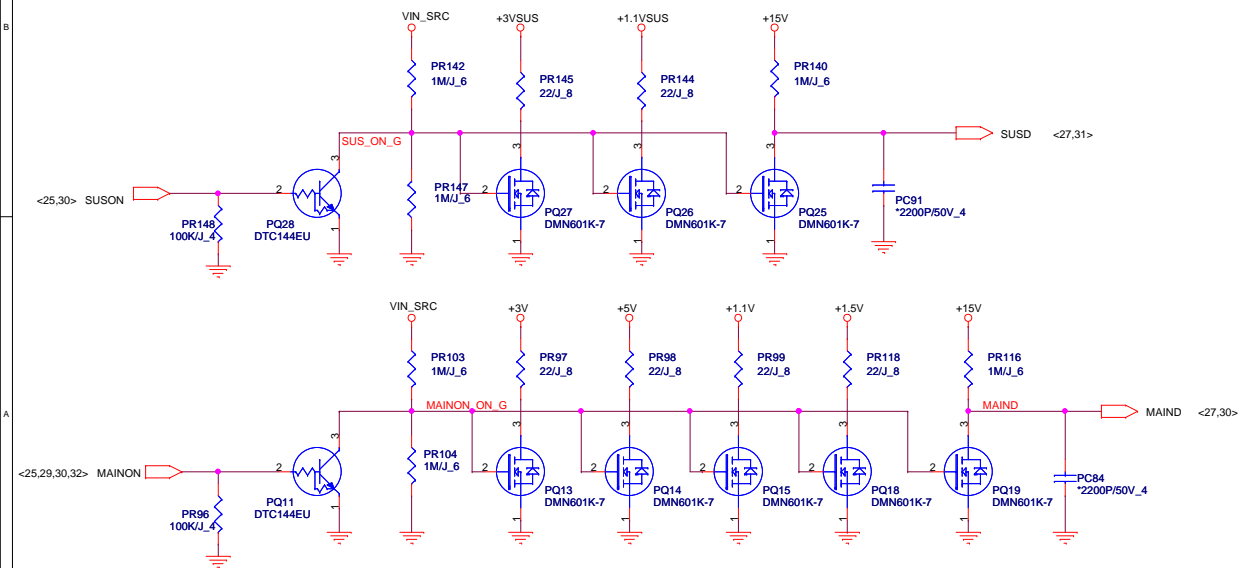
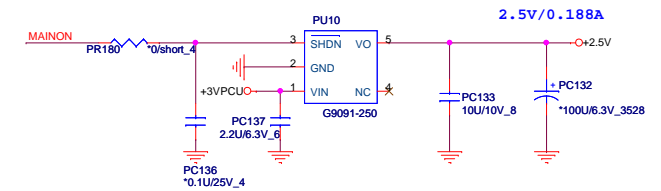
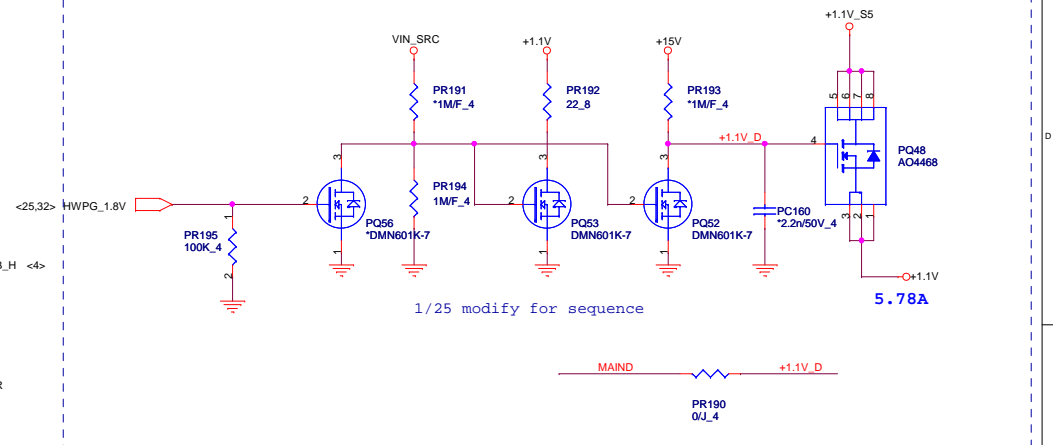
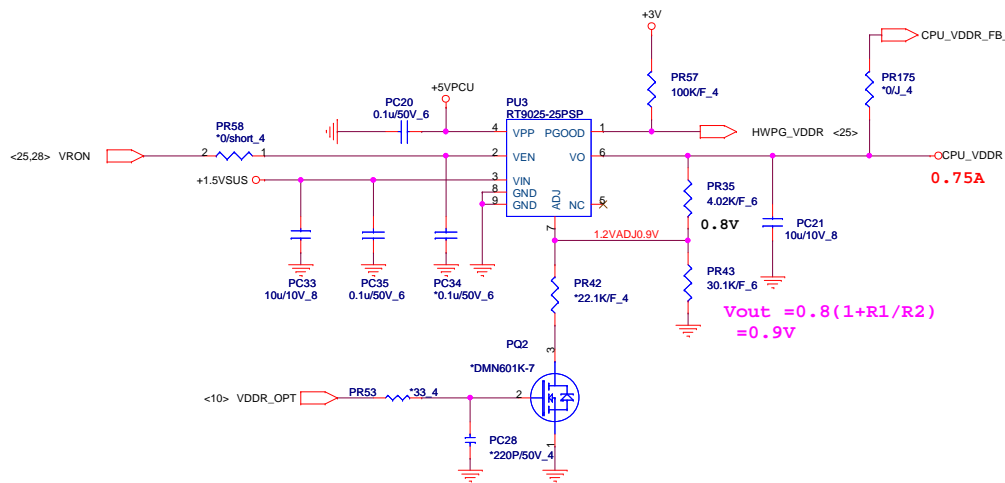
$$L(\text{ripple current}) = (19 - 1.1) * 1.1 / (1u * 272k * 19) \sim 3.81A$$

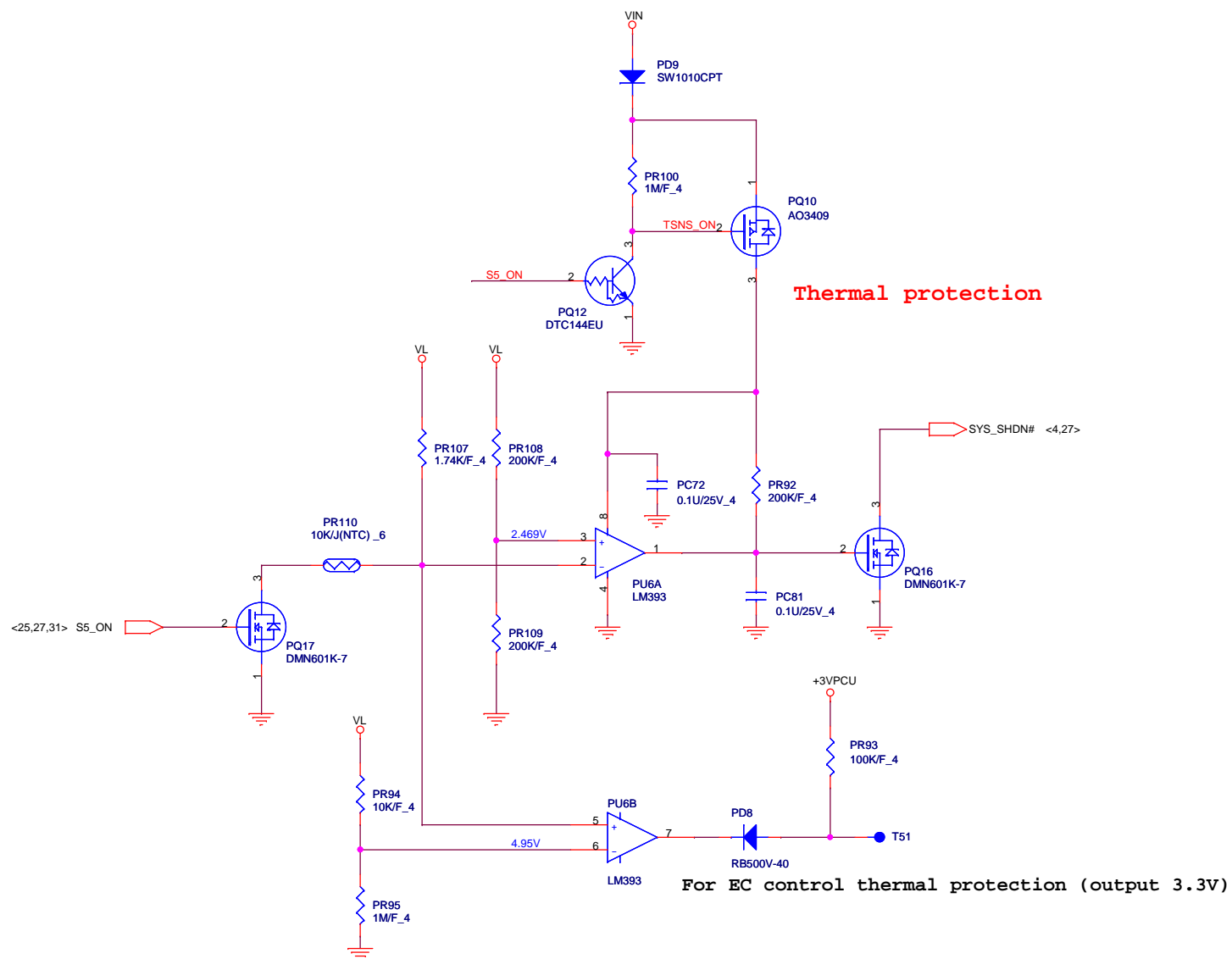
$$13m * 8.5 = R_{ILIM} * 20uA$$


$$R_{ILIM} = 5.49K$$

 <b>Quanta Computer Inc.</b> <b>PROJECT : ZH9</b>		Size	Document Number	Rev
				4A
<b>VCCP 1.1V(UP6111A)</b>		Date:	Sunday, March 28, 2010	Sheet 31 of 40

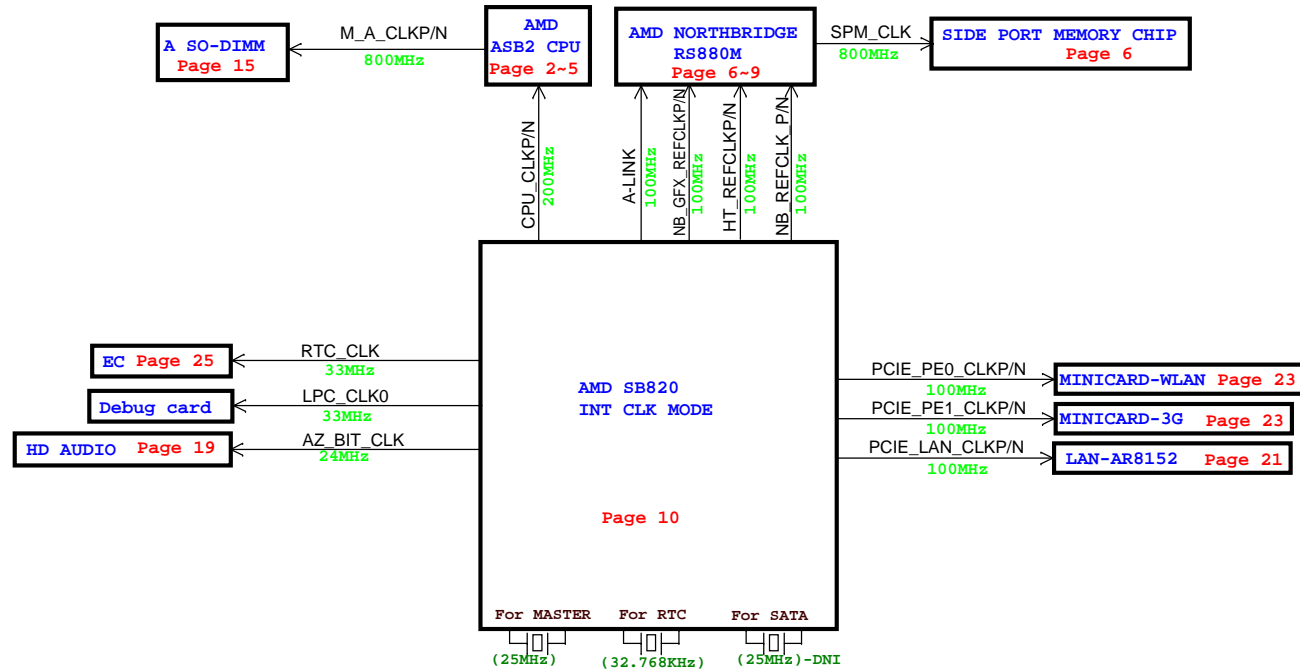






 <b>Quanta Computer Inc.</b> <b>PROJECT : ZH9</b>		Rev
		4A
Size	Document Number	
<b>Thermal protect</b>		
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# INTERNAL CLOCK MODE



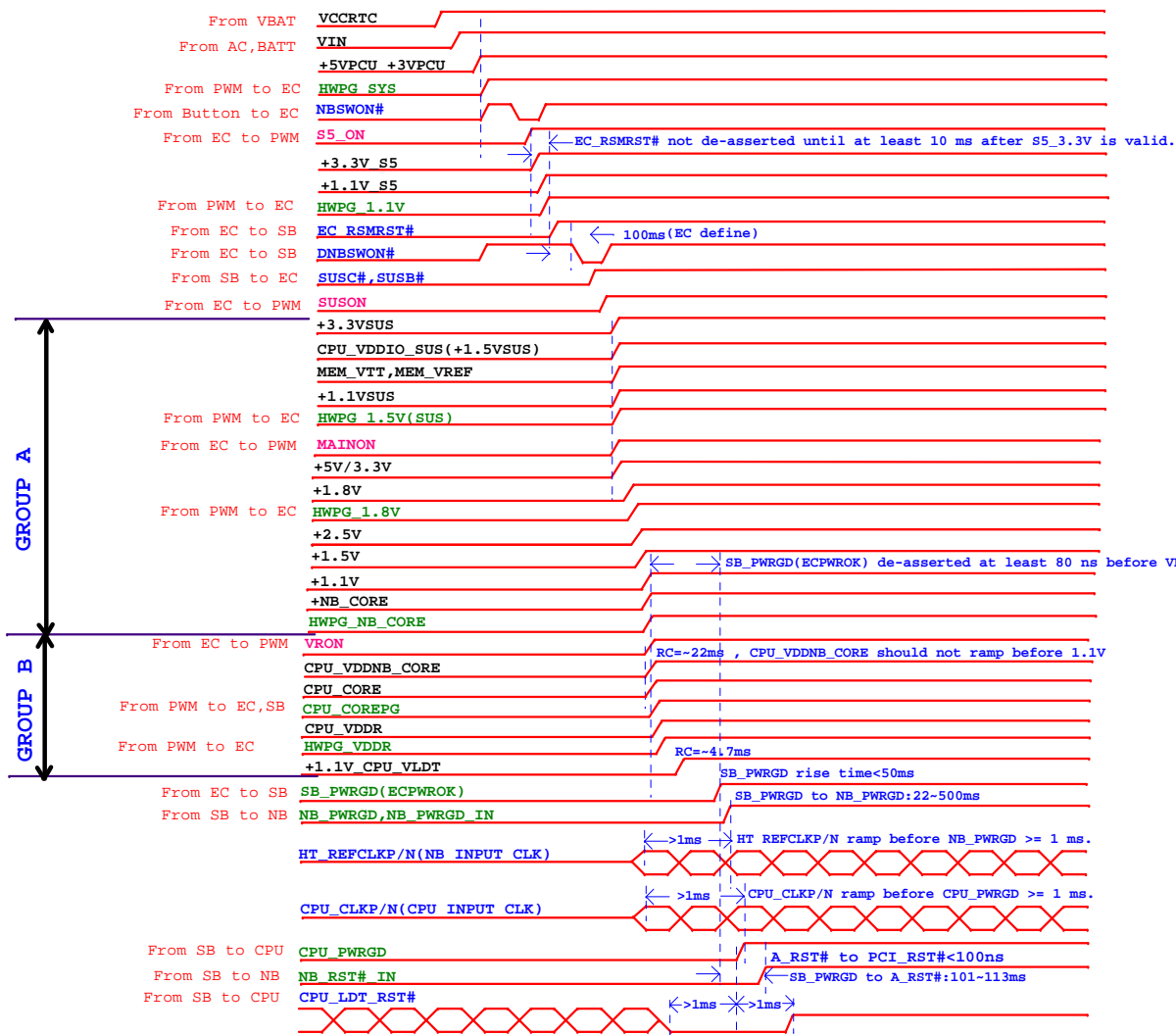
Quanta Computer Inc.

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	<b>Clock Distribution Diagram</b>	4A
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## Nile Power On Sequence



## Power on sequence required:

SB820:

- 1.EC\_RSMRST# ramp up time (10% to 90%) <= 50 ms
- 2.SB\_PWRGD(ECPWROK) rise time <= 50 ms
- 3.SB\_PWRGD(ECPWROK) fail time <= 1 ms
- 4.SB\_PWRGD(ECPWROK) de-asserted at least 1 ns before EC\_RSMRST# is asserted when entering G3 state.
- 5.VBAT will be valid at least 5 seconds before S5\_3.3V and S5\_1.1V are ramped up to allow start time for internal RTC.
- 6.50us<=all power rails rise time except +3.3V\_S5<=40ms
- 7.100us<=+3.3V\_S5 rise time<=40ms
- 8.+1.8V\_S0 rails cannot ramp before the +3.3V\_S0 rails.
- 9.+1.1V\_S0 rails cannot ramp before the +1.8V\_S0 rails.
- 10.+1.1V\_S0 rails cannot ramp before the +3.3V\_S0 rails.
- 11.+1.1V\_S5 rails cannot ramp before the +3.3V\_S5 rails.
- 12.+3V\_S5 ramp down time > 300  $\mu$ s.

RS880:

- 1.+1.1V valid before NB\_PWRGD HIGH >= 1 ms
- 2.+1.8V\_NB\_IOPLLVDD18c(+1.8V) cannot ramp before the 3.3-V rails
- 3.+1.5V\_SPM\_VDDQ(+1.5V) cannot ramp before the 3.3-V rails
- 4.+1.8V\_NB\_VDDLTP18(+1.8V) cannot ramp before the 3.3-V rails
- 5.+1.8V\_NB\_PLLVDD18(1.8V) cannot ramp before the 3.3-V rails
- 6.3.3-V rails cannot exceed the 1.8/1.5-V Sideport or 1.8-V Display and PLL rails by > 2.1 V.
- 7.IOPLLVDD/PLLVDD(+1.1V) cannot ramp up before the 1.8/1.5-V Sideport or 1.8-V Display and PLL rails.
- 8.VDDC(+NB\_CORE) rail cannot ramp before the 1.1-V PLL rails.

## Notice:

- 1.CPU\_LDT\_RST# must be asserted a minimum of 1ms prior to the assertion of CPU\_PWRGD
- 2.CPU\_CLKP/N must be within specification a minimum of 1ms prior to the assertion of CPU\_PWRGD
- 3.CPU\_PWRGD remains deasserted at least 1ms after both CPU\_CLKP/N and all voltages to the processor are within specification for operation
- 4.all NB power rails(1.8V/1.2V/1.1V) valid before NB\_PWRGD at least 1ms
- 5.stable input clocks from CLKGEN(HT\_REFCLKP/N) to NB before NB\_PWRGD at least 1ms

SB SMBUS Table

	CLK GEN	RAM	Mini Card (WLAN)
(SB_DA0)/(SB_CL0) (+3V)	V	V	V
Power Plane	+3V	+3V	+3V
MOS CKT (Level shift)	X	X	X*

\*Reserve: There is not SMBUS function in AVL

EC SMBUS Table

	Battery	CPU thermal Sensor
EC775 SDA1 / SCL1 (+3VPCU)	V	
EC775 SDA2 / SCL2 (+3V)		V
EC775 SDA3 / SCL3 ( )		
Power Plane	+3VPCU	+3V
MOS CKT (Level shift)	X	X

SLP\_S5#(SUSC#):  
S5 Sleep Power plane control - Assertion of SLP\_S5# shuts power off to non-critical components when system transitions to S4 or S5 state.

